
622.08 Mb/s OC-12 ATM-SONET/SDH Reference Design for Multimode and Single-Mode Applications

Application Note 1178

Introduction

The purpose of this application note is to provide design guidance, test techniques, performance data and suggested layout recommendations for a 622 MBd ATM/SONET/SDH physical layer interface reference circuit. This standards-compliant reference design provides a convenient, interchangeable multimode fiber (MMF) or single-mode fiber (SMF) fiber-optic interface via a common interface circuit and component footprint. The fiber-optic transceivers used in this reference design are the 1 x 9 pinout multimode HFBR-5208M and the single-mode HFCT-5208M devices. These fiber-optic transceivers are used with a Vitesse Semiconductor VSC8117 serializer/deserializer/clock recovery/clock generation integrated circuit (SerDes IC) along with a PMC-Sierra PM5355 framer and ATM cell processor IC. With this reference design a designer will be able to copy directly the necessary portion of the circuit and layout for use on a printed circuit board to save product development time, resources and costs. Overall, this reference design is compliant with ANSI T1.646/T1.646a 622 MBd ATM/SONET/SDH standard for multimode and single-mode fiber applications.

As the results show in the **Performance Data** section, this reference design's compliance with the ATM standard's requirements serve the designer well. This reference design's good performance is seen by having a low bit error rate, a small clock recovery window opening, excellent fiber-optic receiver sensitivity, extra margin for the single-mode optical eye-mask, good frequency-based jitter performance for the single-mode fiber-optic transceiver and clock recovery/generation circuitry, etc. Review the **Performance Data** section for details. The main topics of discussion in this note are listed below.

Application Note Topics:

- Introduction
- Circuit Interfaces
- SerDes Comments
- Framer Comments
- PCB Layout
- Performance Data
- Test Methods
- Conclusions
- Appendix

Circuit Interfaces Basic Function of Reference Design

The basic reference design's circuit is of a loop-back configuration. A high-speed, serial 622 MBd optical signal is

sent to the reference design board which it is then converted into high-speed serial data and clock signals. In turn, these signals are converted to 8-bit parallel data by the SerDes IC. The 8-bit data is passed onto the framer IC and processed. The framer output 16-bit bus is looped-back into the framer and this data is passed back to the 8-bit bus for reserializing and retiming the data by an on-board clock generator in the SerDes. The reserialized data is then sent off-board as a serial 622 MBd optical signal.

In addition, this reference design circuit is flexible for various test configurations. For example, the serial data can be looped-back at the input to the deserializer to analyze just the serial portion of the circuit. This is called the Facility Loopback Mode of the SerDes IC. Control signals for the serializer/deserializer can be set to specific conditions to allow various modes of operation or diagnosis. Alternate reference clock inputs can be used for improving low-frequency jitter performance of the SerDes transmit phase-locked loop. Figure 1 illustrates a block diagram of this 622 MBd reference design. Figure 2 shows a picture of this 622 MBd reference design board.

Serial Interface: Fiber-Optic Transceiver and SerDes IC

The high-speed serial interface between the fiber-optic transceiver and the SerDes device is relatively simple and straightforward to design. This section only describes the circuit interface design issues. High-speed signal fidelity concerns and board layout issues will be discussed in the **PCB Layout** section. Figure 3 shows the

simplified interface circuit to use for networking equipment. Figure 3 is a subset of the full reference design schematic shown in Figure 5. Many of the extra circuit options shown in Figure 5 are for evaluation and testing purposes with the reference design circuit for this application note. These extra options are not needed for the normal, physical layer interface circuit.

As shown in Figure 3, the 5 V dc PECL 622 MBd serial data lines to and from the fiber-optic transceiver are directly connected to the SerDes input and output via 50 Ohm differential transmission lines. No additional ac-coupling capacitors are necessary as when 5 V dc to 3.3 V dc interfaces must be done. This is possible because the fiber-optic transceiver is 5 V dc PECL data and the SerDes PECL input/output stages can be internally powered by 5 V dc as well, even though the VSC8117 SerDes is mainly a 3.3 V dc powered device. At the fiber-optic receiver source end of the lines, each output has a biasing resistor of 160 Ohms to ground. This 160 Ohm value provides a low impedance path which quickly pulls-down the emitter follower output. This helps the output fall time be more symmetric with the output rise time to reduce common-mode EMI generation. At the load end of the fiber-optic receiver data transmission lines, there is a 100 Ohm line-to-line resistor that terminates the data at the SerDes input. Similarly, the SerDes data output has source biasing pull-down resistors of 120 Ohms which send PECL signals via 50 Ohm differential transmission lines to the fiber-optic transmitter input stage where another 100 Ohm line-to-line resistor terminates these lines.

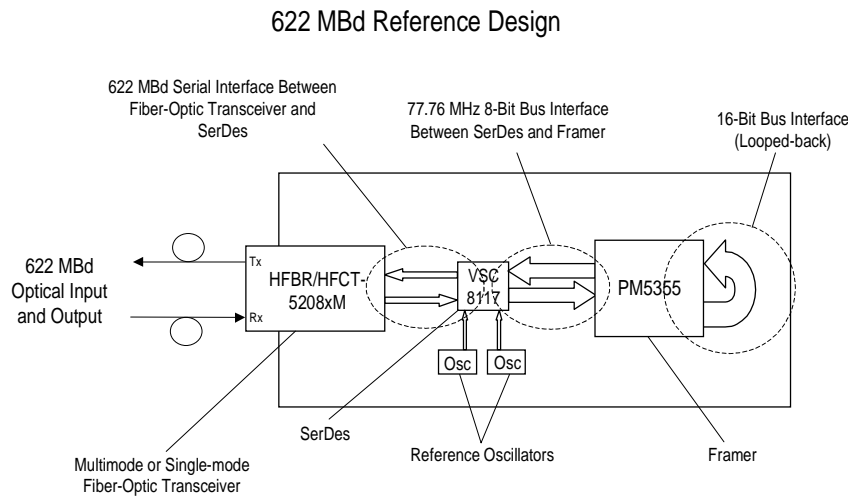


Figure 1. Block Diagram of 622 MBd Reference Design.

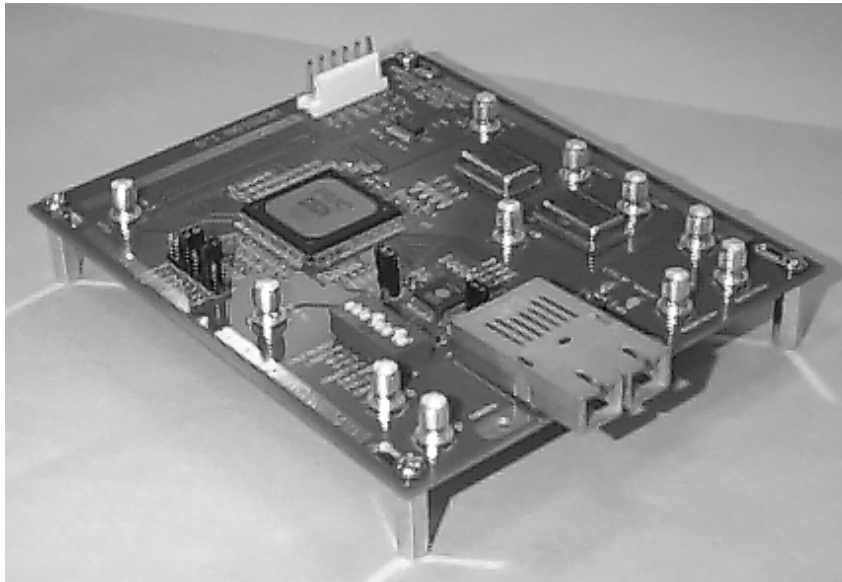


Figure 2. Picture of 622 MBd Reference Design.

The Signal Detect (SD) is connected directly to the SerDes's LOSPECL input via a 50 Ohm transmission line. A 270 Ohm pull-down resistor is needed only at the fiber-optic receiver SD output. Since this line infrequently switches state, power consumption can be saved by not terminating this line in the standard 50 Ohm PECL manner. Even though there is an alternate Loss of Signal circuit provided by the VSC8117 which can be used if the fiber-optic receiver data outputs go to static state levels when the input optical signal is removed, this is not the case with the HFBR/HFCT-5208M transceivers. These receivers will output PECL-level noise chatter, not static data state levels. When the PECL Signal Detect output is permanently connected to the SerDes, the alternate LOS circuit is defeated. More information about this alternate LOS circuit will be mentioned in the **SerDes Comments** section. A 5 V dc PECL-to-TTL translation circuit (MC100ELT23) is provided to light green or red LEDs to indicate whether SD is asserted or de-asserted (receiving or not receiving usable signal) respectively. Typical HFBR-5208M SD de-assert level is approximately -33.4 dBm avg. and asserts at approximately -30.6 dBm avg., yielding a hysteresis amount of 2.8 dB. The corresponding de-assert BER level is in the range of 10^{-3} – 10^{-4} .

The power supply filter circuit for the HFBR/HFCT-5208M is the same for both multimode and single-mode transceivers. There are two identical, but separate, V_{CC} filter circuits used; one circuit for the transmitter section and one for the receiver section. The inductor-capacitor (LC) filter

circuits provide good power supply noise rejection from the board and prevent transmitter-receiver mutual power supply crosstalk as well. These filter components should be located as close as possible to their respective V_{CC} power pins. Ferrite beads used in place of the surface-mount inductors do not provide any substantial low-frequency filtering for these transceivers. The fundamental resonance frequency for the LC filter circuit is approximately 50 kHz and parasitic resonances will occur at higher frequencies depending upon the specific components chosen. Otherwise, this filter circuit substantially attenuates high-frequency noise well past the operating frequency of this circuit. The recommended 1 μ H surface-mount inductors are from TDK Corporation with part number NL322522T-1R0J-3 or equivalent. The 0.01 μ F capacitors on the V_{CC} pin side of the filter should be right next to the pin. All 0.01 μ F capacitors should high-quality, monolithic ceramic bypass capacitors.

Parallel Interface: SerDes and Framer

There are two 8-bit bus circuits and two corresponding byte clock circuits for interfacing between the VSC8117 SerDes and the PM5355 Framer ICs that are shown in Figure 3. The reference design board's transmit data (TXIN) and receive data (RXOUT) 8-bit bus interfaces are slightly simplified for use in a regular application circuit. The simplification removes jumpers in the TXLSCLKOUT and RXLSCLKOUT lines as well as removes 0 Ohm resistors in the RXOUT lines. These 0 Ohm resistors were placeholder resistors for use in dampening

potential ringing on these lines. The individual RXOUT and 8-bit byte clock (RXLSCLKOUT) lines should be 75 Ohms or higher impedance because the output driver stages do not properly support lower impedance lines. Each RXOUT line should be of equal length. The RXLSCLKOUT line length should equal the RXOUT line length as well. Equal line lengths minimize bit skewing on the bus.

The line length is equally important for the TXIN data and TXLSCLKOUT byte clock lines. However, the corresponding POUT line drivers of the PM5355 are capable of driving 50 Ohm lines. Since the TXLSCLKOUT driver needs a 75 Ohm line, it is recommended that all 8-bit bus and clock lines be the same 75 Ohm impedance to minimize bus timing skew. The line lengths for the TXIN/TXLSCLKOUT lines do not need to equal the RXOUT/RXLSCLKOUT lines in length; they only need to match line lengths within each bus.

The interconnecting Frame Pulse signal path from VSC8117 to PM5355 should have the same line length and impedance as the RXOUT/RXLSCLKOUT lines. The zero Ohm resistors in the RXOUT/RXLSCLKOUT lines next to the output pins are placeholders for inserting impedance into the line to help reduce possible ringing effects. Generally, these can be omitted. However, it is good practice to use the 33 Ohm resistors in the TXIN (POUT) lines next to the respective outputs since these lines are driven by CMOS drivers that switch approximately 5 V signals in a short transition time which can cause ringing on the lines.

The 3.3 V dc TTL RXOUT/RXLCKOUT signals are of sufficient signal swing to adequately drive the CMOS TTL PIN 8-bit data bus inputs of the PM5355. Conversely, the VSC8117's TXIN input 8-bit data bus lines are designed to accept the CMOS 5 V dc POUT signals from the PM5355 even though the VSC8117 is powered by 3.3 V dc V_{CC} .

The TCLK jumper is not needed in a normal application circuit. This jumper was used on the reference design for testing purposes.

In the reference design circuit, there are SMA connection points to access the TXLCKOUT and RXLCKOUT signals. Normally, these would not be needed in a typical circuit. See further details about special use of RXLCKOUT signal in the **SerDes Comments** section.

Proper V_{DD} filtering of the SerDes device protects the unit from having marginal or unacceptable data error performance. The V_{DD} power supply pins are bypassed with X7R surface-mount 0.1 μF capacitors. Of the seven V_{DD} power pins, two neighboring pins share a bypass capacitor. The overall V_{DD} is bypassed by a 10 μF capacitor for additional low-frequency V_{DD} noise attenuation.

The two V_{DDP} PECL power supply pins are treated in similar fashion as the V_{DD} power pins. The two V_{DDA} analog power supply pins for the Clock Recovery Unit (CRU) and Clock Multiplier Unit (CMU) Phase Locked Loop circuits are individually filtered for extra V_{DDA} noise rejection. This helps minimize any noise that may add unwanted jitter to the PLL performance. The surface-mount inductor-capacitor

filter circuit (LC) provides a low-bandwidth V_{DDA} filter that arrests noise frequencies over a broad frequency range. These two filter circuits are not just bypassing, but actually filtering the V_{DDA} pins.

All bypassing and filtering circuits should be located as close as possible to their respective power pins for best noise reduction effects. Note that use of a ferrite bead in place of the surface-mount coil inductor in the LC filter will not provide as effective a low-frequency V_{DDA} noise filter circuit as does the coil inductor circuit. The weak-rejection frequency point for the coil inductor LC filter circuit is at its fundamental resonance frequency of approximately 15.8 kHz where the noise rejection is nonexistent and the resonant contributes to make the V_{DDA} noise worst. Otherwise, the LC filter attenuates at twice the rate that a RC bypassing circuit would do.

SerDes Comments

This section outlines different topics of interest about the VSC8117 SerDes application in this design. These comments will help one to understand some of the unique design issues and how best to use the VSC8117 part.

In order to minimize noise coupling into the two analog circuit PLLs within the SerDes IC, the 0.1 μF PLL loop filter capacitors (C2, C3) need to be located very close to their respective pins on the VSC8117. If this is not done well because the capacitor leads are long or a noise source is next to these capacitors, then additional jitter would appear on the recovered clock or the transmit clock. This additional jitter would lead to

suboptimal bit error performance on the received data or poor jitter generation performance for the transmitted data.

The reference oscillator for use with the SerDes IC needs to be carefully selected. For the Clock Multiplier Unit's (CMU) reference oscillator, a crystal oscillator with ± 20 ppm stability needs to be used for public network ATM/SONET/SDH applications. Avoid PLL-based oscillators for this stability requirement.

It is possible to use either a 77.76 MHz or a 19.44 MHz reference crystal oscillator with the VSC8117 on this reference design by changing the appropriate DIP switch settings. It is better to use a higher frequency crystal oscillator for the reference oscillator because there are more transitions from the oscillator to help keep the PLL on frequency. Use a 77.76 MHz crystal oscillator instead of a 19.44 MHz crystal oscillator for standard 622.08 MBd application. In this reference design a 5 V differential PECL, 3rd overtone crystal oscillator was chosen over a single-ended TTL oscillator for better frequency stability performance. As for the Clock Recovery Unit's (CRU) reference oscillator, a simple AC MOS/TTL crystal oscillator works fine since the oscillator is only keeping the CRU operating near the recovered clock's frequency of 622 MHz. This is a less expensive, but adequate, crystal oscillator to use.

The dual-in-line, 8-gang slide switches (S1) are set to their normal control and operating positions for a standard 622 MBd application. Table 1 lists these switch settings.

Table 1. VSC8117 SerDes Operating Mode Default Switch Settings on Reference Design Board.

DIP Switch Number	Label	VSC8117 Pin Number	Switch Status		Operating Mode
			Position	Enabled/Disabled	
1	CRUEQLP	64	ON	Disabled	Loops back 8-bit Input Parallel Data at the Input Serial Data Point
2	FACLOOP	63	ON	Disabled	Loopback Input Serial Data
3	EQULoop	62	ON	Disabled	Loop back 8-bit Input Parallel after being Serialized
4	CRUREFSEL	60	ON	CMU REFCLK	Selects CMU or CRU Reference Clock for CRU
5	STS12	59	OFF	622.08 Mb/s	Select Reference and Output Frequencies for CMU
6	RESET	1	ON	Disabled	Resets Frame Detection, Dividers, Controls
7	LOOPTIM0	2	ON	Disabled	VSC8117 Synchronously Timed by External Clock Source
8	CMUFREQSEL	3	ON	77.76 MHz	Select Reference and Output Frequencies for CMU
2 & 3	SPLIT LOOPBACK	63 & 62	ON & ON	Disabled	Simultaneous Loopback of Serial and Parallel Data

VSC8117 pin voltage & DIP Switch position: "ON" = 0 Vdc (disabled), "OFF" = 3.3 Vdc (enabled)

In this application circuit, the switch labeled "FACLOOP" is a convenient switch for allowing the data from the fiber-optic transceiver output to be serially looped-back at the input clock recovery/data retiming circuit of the VSC8117 unit back to the fiber-optic transceiver input ("OFF" position). When the FACLOOP switch is in the "ON" position for normal application circuit use, the serial data from the fiber-optic transceiver is sent onward to be de-serialized, and then past on to the framer IC. For a complete functional description of these switches, refer to the Vitesse Semiconductor VSC8117 data sheet.

The VSC8117 IC has a Loss of Signal (LOS) detection circuit that can be used to:

1. Monitor serial data activity
2. Determine if data activity has ceased for a determined period of time (no transitions for more than 128 bits)
3. Indicate a LOS existence
4. Flag the Framer IC of LOS state by causing the 8-bit bus to go to an all-zeros condition.

This LOS feature can be used if the Signal Detect (SD) signal from the fiber-optic receiver is not connected at the VSC8117 LOSPECL input and the fiber-optic receiver data lines can become inactive for a sufficient length of time. If both the LOS and SD features are used together, the SD will dominate. This is because there will always be activity on the serial data path from the fiber-optic receiver, with or without an input optical signal being present. In the reference design circuit, the LOS feature

(LOSDETEN_) can be switched off via a jumper. In normal applications with these components, the SD signal is used and not the LOS circuit.

The VSC8117's RXLSCKOUT 8-bit byte clock can be used as a 77.76 MHz clock source for an external, very low loop-bandwidth 77.76 MHz PLL circuit. This RXLSCKOUT signal is available via a SMA connector on the reference design board. In turn, the output of the external, low loop-bandwidth PLL circuit is used to supply the VSC8117 Clock Multiplier Unit (CMU) REFCLK input in place of the on-board PECL 77.76 MHz crystal oscillator. This low bandwidth filtered REFCLK 77.76 MHz signal is internally multiplied by a factor of eight to transmit the serially-timed output data at 622.08 MBd. This low loop-bandwidth 77.76 MHz PLL improves jitter transfer performance of the VSC8117. In this configuration,

the CRUREFSEL must be set (S1, #4: CRUREFSEL=OFF) for the Clock Recovery Unit (CRU) to use its separate CRUREFCLK input crystal oscillator. Contact Vitesse Semiconductor Inc. for more details regarding an external, low loop-bandwidth PLL circuit. Also for convenience, the TXLSCKOUT 8-bit byte clock is available via a SMA connector on the reference design board for a trigger or a transmit byte-clock monitoring point.

Since there is no external clock recovery circuit used in this application, the VSC8117 RXCLKIN± are not used; hence, RXCLKIN- is connected to ground via a pull-down resistor. Also, DSBLCRU is grounded in this application to enable the CRU. DSBLCRU would need to be pulled high to disable the internal CRU and allow an external 622.08 MHz recovered clock to be used.

An optional REFCLK (TTL) input is available for use as the reference oscillator input for the VSC8117 Clock Multiplier Unit should the PECL REFCLKP± oscillator not be used. This REFCLK input is accessible via the REFCLK SMA connector on the reference design board.

Comment on Dual Rate Applications (155 MBd / 622 MBd)

Some designers would be interested in using this reference design circuit for a dual data rate application, i.e., operate at either 155.52 Mb/s (OC-3) or 622.08 Mb/s (OC-12). Although the HFBR/HFCT-5208M, VSC8117 and PM5355 can operate at either data rate, performance of the HFBR/HFCT-5208M is only guaranteed at 622 MBd. At issue is the fact that the multimode HFBR-5208M receiver will not provide a

sensitivity of -30 dBm avg. at 155 MBd which is a requirement of the 155.52 Mb/s OC-3 ATM-SONET/SDH standard. The HFBR-5208M sensitivity is specified at -26 dBm avg. In addition, the PM5355 requires a microprocessor controller to operate at other than 622.08 Mb/s. If a non-compliant application is acceptable for the 155.52 Mb/s use, then there is the possible opportunity to use this fiber-optic transceiver, the SerDes and Framers ICs appropriately to achieve this dual-purpose goal.

Framer Comments

Exercise care when interconnecting the PM5355 framer/ATM cell processor and the VSC8117 SerDes device via the 8-bit bus, or when interconnecting the 16-bit bus to and from the next level IC. The design care that is taken will prevent excessive timing skew from occurring either between the respective byte clock and the bus data lines or between data line to data line. The data and byte clock lines should be matched in length and in impedance value. For example, the setup and hold times for the 16-bit bus data lines must be satisfied to allow the bus signals to be properly clocked into the PM5355. In the reference design circuit, the 16-bit bus is looped-back with bus lines of equal length and equal impedance. The TFCLK (byte clock) meets the required setup and hold timing for this clock input relative to the bus data lines.

The 16-bit bus is clocked out of the PM5355 by RFCLK and the 16-bit bus is clocked into the PM5355 by TFCLK. These clocks need to operate fast enough to prevent the respective input and output registers from

overflowing. Both of these clock signals must not operate beyond 52 MHz.

On the reference design board are two options for supplying these clocks:

1. The RFCLK and RFCLK signals can be provided independently via two separate SMA clock inputs.
2. An external RFCLK signal is supplied to the RFCLK SMA connector. An on-board inverter option is used to create TFCLK. The setup and hold times of the 16-bit data bus input (TDAT#) are met with the rising edge of TFCLK. This TFCLK rising edge occurs after RFCLK rising edge by the combined half period of RFCLK, plus the propagation delay of the inverter device and the delay of the printed circuit board trace.

There are eight header pins on the reference design board for the PM5355; six are for monitoring signals and two are for jumper connections of this IC. The monitoring header pins must not be jumpered (shorted) together. These pins are TXPRTY0, TXPRTY1, TSOC, GROCLK, GTOCLK, FPOUT. The two jumper connections are RSOC and TLAIS. For example, the jumper for TLAIS, when opened, will cause an alarm to be inserted into the data which would be recognized by the receiving portion of a PM5355 to indicate a specific alarm was used to alert or test a subsequent circuit. With regard to these eight header connections, please consult their specific detailed explanations found in the PM5355 data sheet.

Four red LEDs are operated by the PM5355 on the reference design board. Two LEDs monitor the status of the SONET/SDH framing. They are labeled Loss of Frame (LOF) and Out of Frame (OOF). When the PM5355 is provided a valid SONET/SDH frame these LEDs will be off. If the frames are not correct or missing, these LEDs will be turned on. There is a Loss of Signal (LOS) LED that is turned on when the PM5355 determines that a valid loss of incoming signal has occurred (20 μ s \pm 3 μ s of consecutive all-zeros condition on the 8-bit bus input). Also, the LAIS LED will light when an alarm (111 pattern is detected in bits 6, 7, and 8 of the K2 byte for 3 or 5 consecutive frames) is inserted into the data. This LAIS alarm can be tested on the reference design board circuit by opening the TLAIS jumper when the fiber-optic transceiver is fiber looped-back on itself. The PM5355 generated Idle cells are replaced with the inserted alarm and the LAIS LED will then light.

As mentioned in the **SerDes Comments** section, the 8-bit bus interface between the SerDes to the PM5355 framer (3.3 V TTL to 5 V TTL) has sufficient 3.3 V TTL signal swing to operate the 5 V TTL input properly. Also, from the PM5355 framer to the SerDes (5 V TTL to 3.3 V TTL), the SerDes's 3.3 V TTL input is 5 V TTL tolerant. In addition, the 5 V TTL 16-bit and 8-bit bus signals from the CMOS PM5355 framer outputs uses a 33 Ohm resistor to help reduce ringing on these lines due to the fast 5 V logic transitions. For more in-depth information about the PM5355 Framer IC, consult its complete data sheet at PMC-Sierra's web site: www.pmc-sierra.com.

PCB Layout

General Guidance

The following information for the printed circuit board layout is listed in the next topic sections. The reference design circuit board followed these recommendations and achieved a working circuit board from the first layout. Additional details on the reference design board layout and construction are given in the **Appendix** section of this note.

Signal Fidelity

- 1) For the 622 Mb/s high-speed serial data lines, position the fiber-optic transceiver and SerDes devices reasonably close together - an inch (25 mm) or so is commonly done. Use either microstrip or stripline techniques to create differential 50 Ohm characteristic impedance transmission lines for the data paths. Regardless of how short the data paths may be, always design them as transmission lines of low characteristic impedance to help control parasitic effects from adversely affecting the circuit performance.
- 2) Keep the differential transmission lines of equal length to minimize pulse-width distortion and time skew. Route these lines together to avoid unequal crosstalk coupling. Avoid 90° bends in the transmission line traces. Instead, use uniform radius curves or 45° bends to minimize impedance discontinuities on the lines. Avoid unbalanced, or single-ended, use of differential lines to prevent introducing unwanted pulse-width distortion.
- 3) Properly terminate transmission lines with a load impedance equal to the characteristic impedance of the

line at the end of the line where the signal is to be used by the input of the follow-on device. This helps minimize reflections (ringing). Less ringing keeps the data eye-opening wide and contributes to less EMI emissions. Keep biasing resistors on the output of the fiber-optic transceiver and the output of the SerDes unit close to the source end of their lines.

Should differently powered PECL logic be interfaced, e.g., 5 V PECL interfacing with 3.3 V PECL, then ac-coupling capacitors are used in the high-speed, serial data lines. Place these capacitors and any vias in these lines at the source end or at the load end of the transmission line; do not place either of these items in the middle of the lines. Use surface-mount components, typically of 0603 package size, to minimize parasitic effects from influencing the circuits.

- 4) Use of continuous power and ground planes is essential for best noise performance. Generally, avoid gaps, or special cuts, in the ground planes unless specifically recommended to do so by a component supplier. Ground each V_{SS}, V_{EE} component pin individually to its respective ground plane; do not daisy-chain the ground pins together and then ground the combination of pins at one point. Also, avoid use of sockets for 622 Mb/s signals, unless the sockets are necessary for testing or evaluation purposes. Sockets were used on this reference design board to allow interchanging fiber-optic transceivers as well as reference frequency crystal oscillators. Multilayer boards are a necessity for signal interconnections.

5) Component power pin bypass capacitors must be carefully placed. First, and best to do if possible, a 0.1 μF or 0.01 μF bypass capacitor should be placed directly across the V_{CC} (or V_{DD}) leads and its neighboring ground leads. This bypass capacitor location is on the same side of the board where the component leads are located. The bypass capacitor location is then nearest to the leads, and any traces and vias that are used to connect to the respective V_{CC} or ground planes must connect after the capacitor. If this placement is not possible, then the bypass capacitor should be a 0.1 μF capacitance value and not a 0.01 μF value. The larger bypass capacitor value helps prevent the added trace and via inductance from canceling a significant portion of the 0.01 μF bypass capacitance.

6) When the parallel bus traces are interconnected between the SerDes and framer ICs or between the framer IC and an upper level IC, the individual data and associated byte clock lines must be close to the same lengths as possible to avoid timing skew effects. Length and impedance of data and byte-clock lines may be limited because of either setup and hold-time constraints at a bus input or they are limited by the output stage to drive a line adequately. On the reference design board the 8-bit and 16-bit bus data and byte-clock lines were matched in length and impedance as best as possible.

7) For the analog 3.3 V dc V_{DDA} power supply of the VSC8117 SerDes unit, a small island in the 3.3 V dc power plane was made to separate the digitally noisy 3.3 V dc power plane from this LC-filtered V_{DDA} connection for the

on-board clock recovery and clock generation PLL circuits. This analog 3.3 V dc island is quite small in size and does not interfere with the main 3.3 V dc power plane.

Mechanical Aspects

This reference design board has some mechanical options that can be used to help perform measurements with this board. They are listed below.

Both sides and back edge of the board (power supply connector end) have signal ground strips for convenient ground contact points or to provide an ESD ground path where touching or handling of the board usually takes place.

The front edge of the board where the fiber-optic transceiver is located has four large pads of metal (two on the top surface and two on the bottom surface) that connect to the front mounting posts of the fiber-optic transceiver. The pads have additional holes in them for mounting a chassis bracket or front equipment panel to this board. These pads are not connected to the signal ground of the reference design circuit. The pads are islands of metal for connecting to a chassis. The front mounting posts of the fiber-optic transceiver contact the metalized housing of the fiber-optic transceiver. This post-to-metalized housing connection is not a consistent connection path. For proper connection to the metalized housing an optional, external metal EMI shield provides the correct connection from metalized housing to equipment chassis. These shields are available in a flush-mount style or as an extended-mount style with the metalized housing fiber-optic transceiver.

The four metal standoff legs of the reference design board are mounted into four metal slots which are not connected to anything. These slots allow the reference design board to adjust its position within an enclosure so that either a flush-mount or an extended-mount EMI shield can easily fit to an aperture in the enclosure. Different EMI tests then can be performed more easily.

The fiber-optic transceiver and the reference frequency crystal oscillators are pin socketed for convenient changing of units. In addition, the crystal oscillators have dual footprints for use with either through-hole pin-out or for surface-mount packages. A number of crystal oscillator manufacturers provide compatible pin-out and package sizes for second source use. See the Bill of Materials list in the Appendix.

Artwork, Gerber Files and Schematic

This 622 MBd 1 x 9 multimode or single-mode fiber-optic transceiver/SerDes/framer reference design board is a six layer printed circuit board made from common FR-4 material. The specific layer organization, construction and Bill of Material list for the board are given in the **Appendix, Table A1**, section of this note. Also, in the **Appendix** section is a brief explanation of how to establish microstrip and stripline transmission lines with a specific characteristic impedance for a printed circuit board layout. The transmission line impedance formulas are given for convenient reference. More details on printed circuit board transmission line design can be found in any engineering textbook for layout

design or from general design guidance information in ECL databooks. See **Appendix** for references.

Gerber photo-plotter files for the layout artwork of this reference design can be found on the Agilent fiber-optic web site. These collection of files include all the pertinent information for silkscreen, solder mask, layers 1-6, drill mask and sizes, etc. to develop this version 1.1 printed circuit board. With a gerber photo-plotter editor, this layout can be copied and edited to achieve an optimal layout unique to a designer's requirement. The file name is refdes2.zip. If a designer is using Advanced PCB and Advanced Schematic from Protel Technology Pty Ltd.™ which is a printed circuit board layout and schematic capture software application, then the Protel artwork layout file can be used directly. The Protel file names are refdes2.PCB for the layout artwork and ref_des14G.sch for the schematic. Check the starting URL of www.semiconductor.agilent.com for latest information.

In addition, at the above web site, there are test patterns available for SONET STS-12 and SDH STM-4 for use with Agilent HP 70000 Series Bit Error Tester equipment. These two files are named Hppat05.dat and Hppat09.dat respectively.

Figure 5. shows the complete 622 MBd 1 x 9 multimode or single-mode fiber-optic transceiver/SerDes/framer reference design circuit.

Performance Data

This section presents measured results from the reference design board. The main measurement test points are shown in Figure 4. At each illustrated test point, the “where, what, and why” are explained to help understand the observed performance. It is hoped that this breakout of signal test points gives the designer a better appreciation of the individual as well as the combined performance of reference design components. Throughout these tests typical components and normal operating conditions (room temperature, nominal power supply) were used. The results given in this section will represent what a designer typically should see when measuring an actual interface circuit board. Worst-case conditions or devices were not used for measurement in this section.

The main test data patterns used for these measurements were
 1) a continuously repeating 622.08 Mb/s STS-12 pattern with PRBS 2^7-1 payload or
 2) a SONET/SDH STS-12 pattern with a payload of scrambled ATM cells. The STS-12/PRBS pattern is 77,760 bits in length.

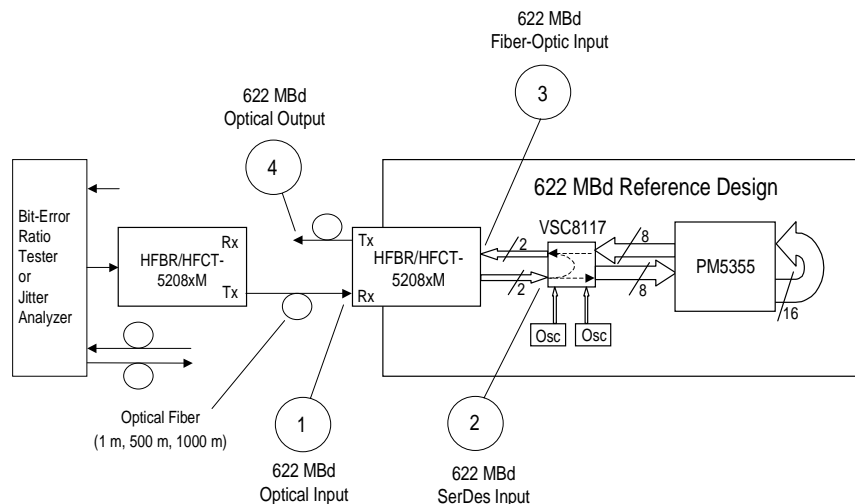


Figure 4. Block Diagram of Measurement Test Points for the 622 MBd Reference Design.

Test Point 1: Optical Stimulus Waveforms

Waveforms of the optical sources used to test the reference design board are shown in Figures 6, 7 and 8. The three optical waveforms for 62.5/125 μm multimode fiber illustrate the effects of fiber dispersion upon the optical signal (longer rise/fall times, less amplitude with increasing length). These three multimode waveforms include the optical losses from the fiber-optic attenuator, various connector adapters and splitter used in the test system, approximately 4 dB total loss.

Figures 9 and 10 show waveforms of the single-mode optical source over 1 m of single-mode fiber: Figure 9 shows a waveform without a 622 Mb/s SONET/SDH filter and Figure 10 shows the waveform with the 622 Mb/s SONET/SDH filter along with a mask template. In general, single-mode waveforms are measured with a standard SONET/SDH 622 Mb/s filter to eliminate the turn-on relaxation oscillation natural to the laser source dynamic response.

The 622 Mb/s OC-12 SONET/SDH filter is a fourth-order Bessel-Thompson filter that has a -3 dB bandwidth of 467 MHz (0.75 x bit rate). Note that the shape of the output optical waveform indicates that the serial input signal provided to the fiber-optic transmitter is properly terminated and replicated in optical form. The 622 MBd ATM-SONET/SDH standard defines an optical eye-opening mask test that must be met by the fiber-optic laser transmitter.

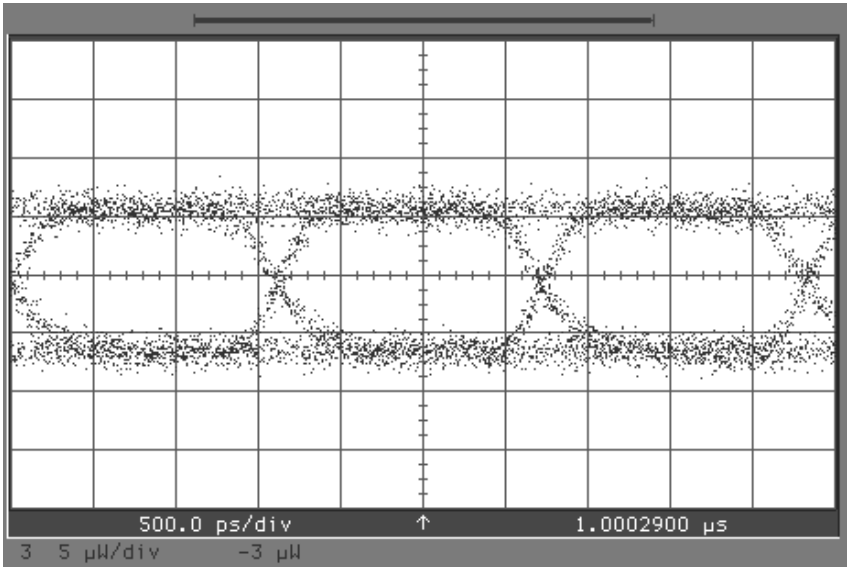


Figure 6. Input Optical Waveform with 1 m of 62.5/125 μm multimode fiber.

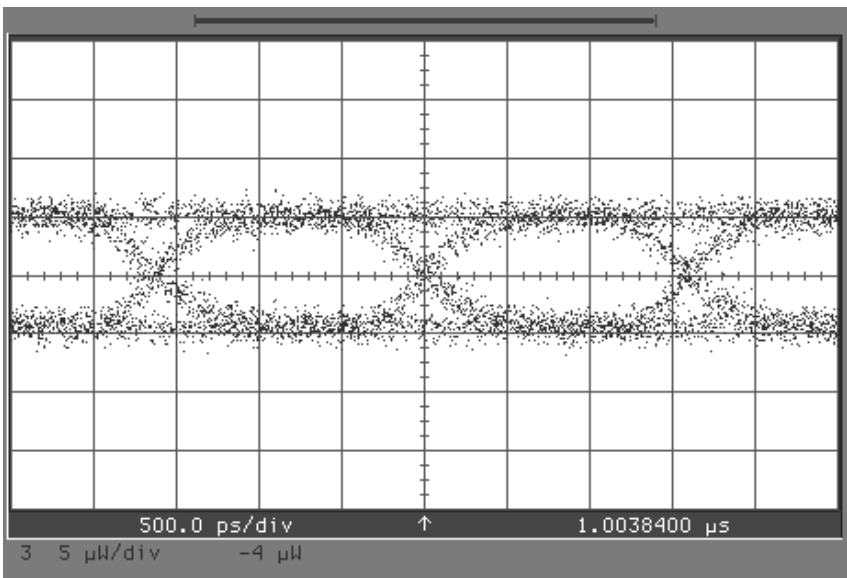


Figure 7. Input Optical Waveform with 500 m of 62.5/125 μm multimode fiber.

Figure 10 displays a typical HFCT-5208M transmitter optical waveform and the 622 MBd ATM-SONET/SDH eye-mask using 1 m of single-mode fiber cable and transmitting the STS-12 test pattern. This mask test has an added mask margin measurement shown. The margin amount is 25% larger than the required mask area. This additional margin area makes it more demanding for the optical waveform to meet the larger keep-out areas. No violations, or “hits”, resulted within the eye-mask template and its margin areas. This result provides more performance capability for the designer to use.

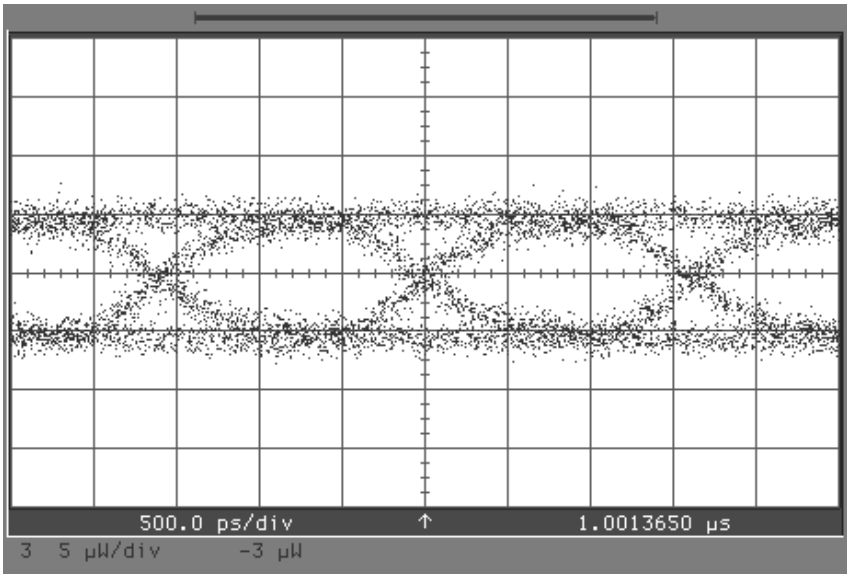


Figure 8. Input Optical Waveform with 1000 m of 62.5/125 μm multimode fiber.

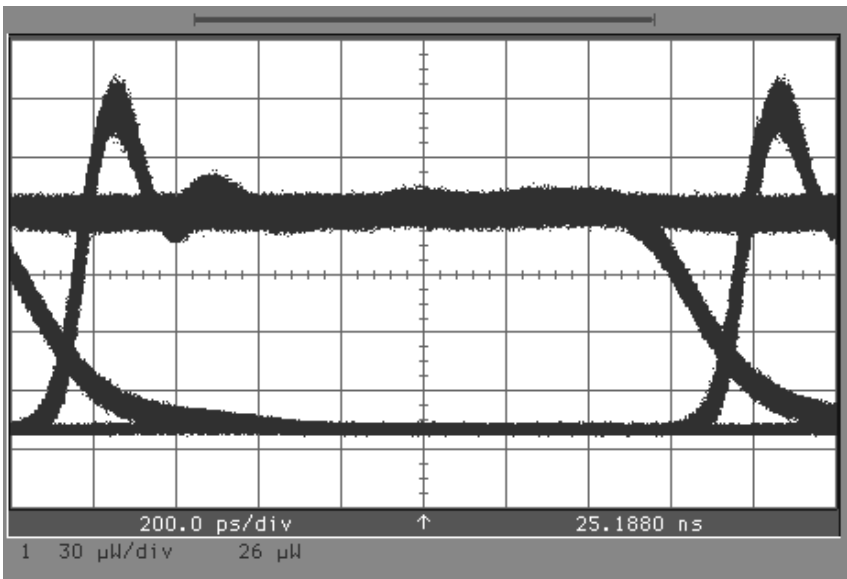


Figure 9. Input Optical Waveform with 1 m of Single-mode Fiber without an OC-12 Filter.

Test Point 2: SerDes Serial Input Data Waveforms

At Test Point 2, waveforms were measured for Data and Data-bar individually and then together differentially for the SerDes VSC8117's serial data inputs. The HFBR-5208M fiber-optic receiver Data/Data-bar outputs supply these signals via 50 Ohm transmission lines to the differential 100 Ohm load termination that is across the VSC8117's inputs. The input optical power to the receiver is set at two conditions: the highest optical power available from the test system and at the minimum sensitivity specification of -26 dBm avg. for this product to meet the multimode 622 MBd ATM-SONET/SDH standard requirement.

For example, at the highest available input optical power level (P_R) to the receiver of $P_R = -22.0$ dBm avg. while using 500 meters of typical 62.5/125 μm fiber, the single-ended Data eye-opening is wide. For this condition, the typical signal-edge jitter is 300 ps peak-to-peak per the oscilloscope's accumulated sample data (~ 113 khits). When the input optical power is lowered to the minimum receiver sensitivity specification of $P_R = -26.0$ dBm avg, per the multimode 622 MBd ATM-SONET/SDH standard, the total Data-edge jitter increases to 400 ps p-p (~ 108 khits). This 400 ps jitter is well within the standard's allowed total edge jitter of 1298 ps peak-to-peak.

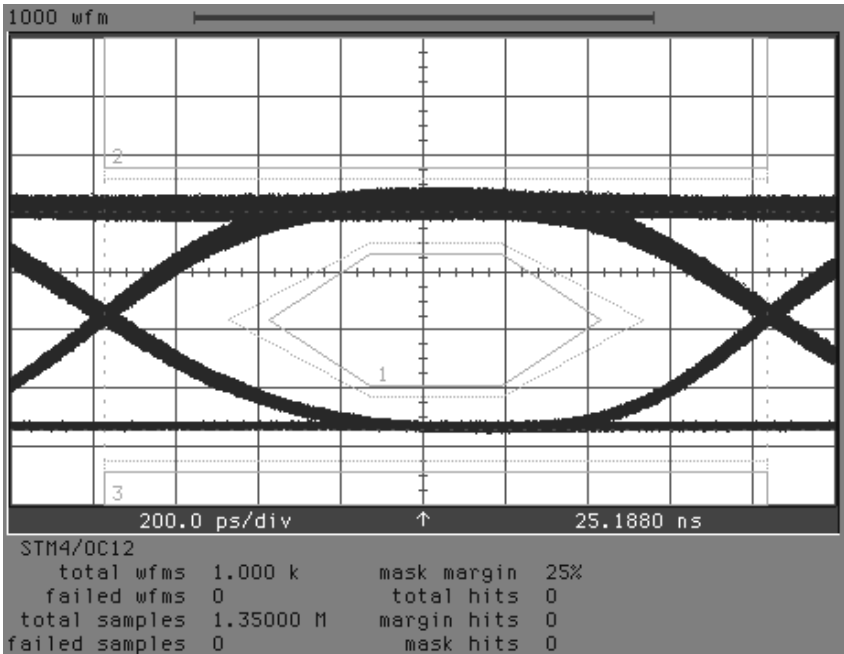


Figure 10. Input Optical Waveform with 1 m of Single-mode Fiber with the SONET/SDH OC-12 Filter and Mask with an additional 25 % Margin.

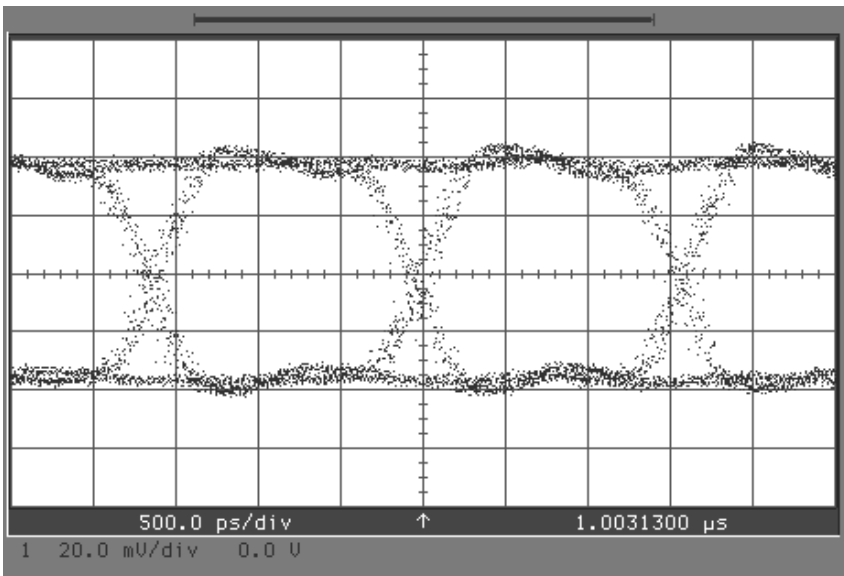


Figure 11. SerDes Serial 622 MBd Data Input with 500 m of 62.5/125 μm fiber and at $P_R = -26$ dBm avg.

Figures 11, 12 and 13 show respectively the Data, Data-bar and differential Data eye-openings at the SerDes data inputs for the input optical power level of -26 dBm avg. These waveforms were measured with an approximate 10:1 resistor divider that is completed by a 50 Ohm input to a high-speed, sampling scope (20 GHz bandwidth). Figures 11 through 13 show clean, wide eye-opening waveforms that have negligible signal reflection effects in them. Table 2 shows total data jitter measured at $P_R = -26$ dBm avg. by histogram method and “Tub” method vs. fiber-optic link length.

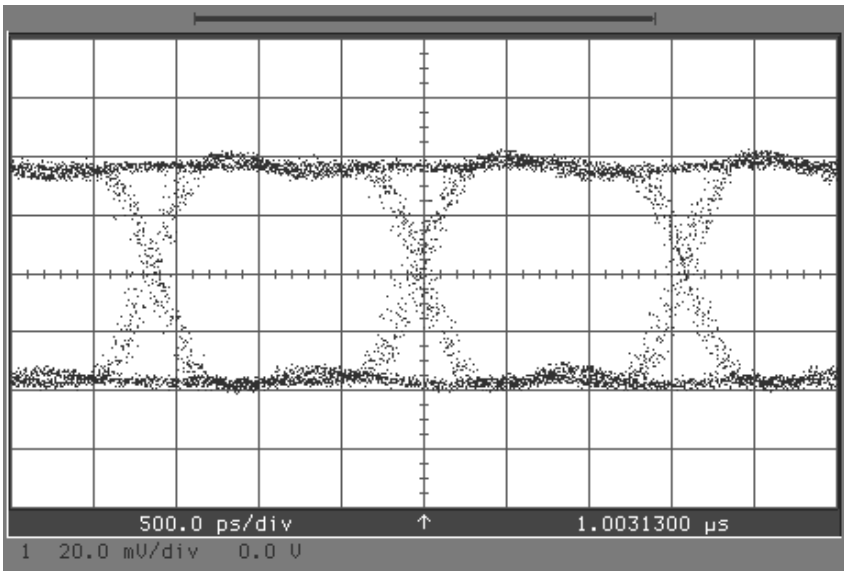


Figure 12. SerDes Serial 622 MBd Data-bar Input with 500 m of 62.5/125 μ m fiber and at $P_R = -26$ dBm avg.

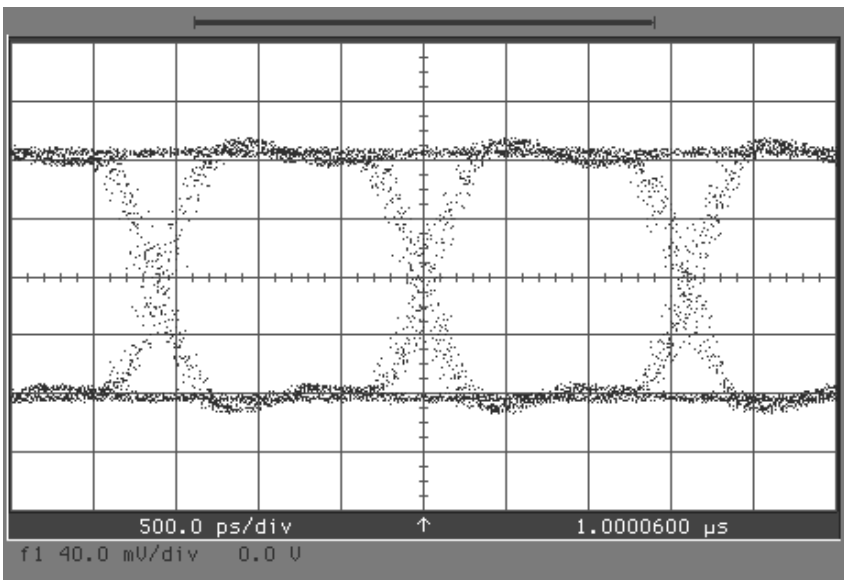


Figure 13. SerDes Serial 622 MBd Differential Data Input with 500 m of 62.5/125 μ m fiber and at $P_R = -26$ dBm avg.

Table 2. Total Data Jitter Measured at $P_R = -26$ dBm avg. by Histogram Method and “Tub” Method vs. Fiber-Optic Link Length.

Link Length metres	Total Data Jitter (Histogram) $P_R = -26$ dBm avg. ps p-p	Total Data Jitter (Eye Closure at BER= 10^{-10} from Figure 14) $P_R = -26$ dBm avg. ps p-p	Total Data Jitter ANSI T1.646a MMF Standard ps p-p
1	378	463	N.A.
500	400	489	1298
1000	433	532	N.A.

N.A. = Not Applicable

While a sampling oscilloscope provides a convenient way to measure jitter of signal waveforms on a sampled basis, a more accurate method is to check bit-for-bit error performance by using a Bit Error Ratio Tester (BERT). The BERT can be used to develop unique data to help better quantify the jitter performance of a circuit. To use a serial BERT, the Data output from the fiber-optic receiver is connected to the BERT as well as to the SerDes input. This connection allows measurement of the sensitivity of the fiber-optic receiver (P_R) as a function of the BERT's receiving clock time position (t_{sampling}) within the Data eye-opening for a constant bit error ratio condition. When P_R versus t_{sampling} is plotted, the graph is referred to as a "tub" diagram due to its U-shape appearance. In Figure 14, four different curves are given; the three BER = 10^{-10} curves of different fiber cable lengths are derived from a linear regression of higher error-rate data points. The fourth BER = 10^{-6} curve is actual measured values for the 500 meter length of cable. Of these four curves, three different 62.5/125 mm multimode fiber lengths are shown: 1 m, 500 m and 1000 m. The fourth curve of BER = 10^{-6} for 500 m length is used as a quick reference curve to estimate receiver performance without involving lengthy test time. The typical dB difference in the fiber-optic receiver Input Optical Power between BER of 10^{-6} and BER of 10^{-10} for a 500 m link is approximate 1.6 dB at center of the bit interval. How to measure "tub" diagrams is explained later in the **Test Methods** section.

The interesting and informative nature of these tub diagrams is that one figure shows the eye-opening time amount of a data signal for a given input optical power level to a fiber-optic receiver at a required BER condition. The input optical power penalty (dB) can be seen easily if a wider data eye-opening is needed for clock recovery circuit. Since this is a bit-for-bit error measurement, the converse of eye-opening can be determined, i.e., the amount of eye-closure or the total jitter that is occurring on the signal at a specific BER condition. The wider the U-shape tub, the better the eye-opening performance of the fiber-optic receiver. The deeper the U-shape tub, the more sensitivity the receiver is for using less input signal level. Any asymmetry in the U-shape can point to possible design or performance issues. The "tub" diagram is quite an informative figure.

Estimation of SerDes's Input Clock Recovery Eye-Opening Requirement

In the multimode 622 MBd ATM-SONET/SDH standard, the smallest allowable data eye-opening time for the SerDes clock recovery unit to operate within is 310 ps. This is referred to as a time "window" opening needed by the SerDes to recover the clock and retime the serial data without exceeding the required error rate for this application. The VSC8117 SerDes data sheet does not specify this parameter. The following test method and result give a realistic estimate of the actual clock recovery circuit's window opening value.

The VSC8117 SerDes is configured to operate in Facility Loopback mode (FACLOOP switch placed in the "off" position). This mode causes the 622 MBd serial data to loopback from the received data to the transmitted data. The BERT receives this transmitted serial data and then compares its sent data with this returned data. When the BERT's receive clock is

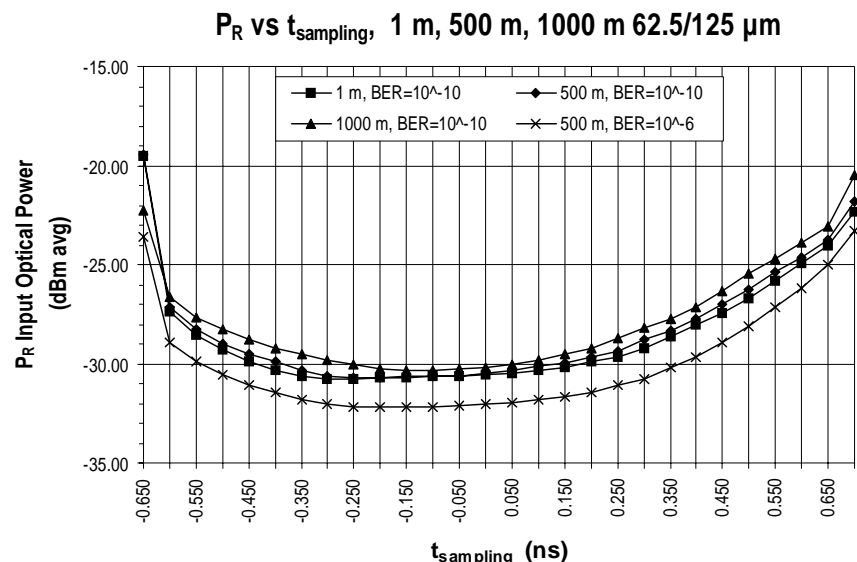


Figure 14. Input Optical Power (P_R) vs. Clock Sampling Time Position (t_{sampling}) at Constant BER of 10^{-10} and 10^{-6} for 1 m, 500 m and 1000 m links - "Tub Diagrams".

positioned at the center of the baud interval of the returning data, the input optical power to the fiber-optic receiver is lowered to different levels to achieve different BER values. This data then is extrapolated by the linear regression technique described in the **Test Methods** section about measuring tub diagrams. A predicted value for the input optical power to the receiver is obtained for a BER of 10^{-10} . This SerDes retimed data error condition of 10^{-10} corresponds to a fully-jittered, or closed retimed data eye. This condition occurred because the input received data eye-opening to the SerDes's input equaled the window opening needed by the clock recovery circuit for the BER of 10^{-10} . The input optical power level that caused the SerDes output to have a BER of 10^{-10} is the sensitivity level used to determine the eye-opening from the corresponding tub curve for the received data at the SerDes input (at the same conditions of BER, cable length, etc.). It is assumed that the clock of the clock recovery circuit is positioned at the center of the baud or data interval. The resulting time-width to the nearest edge of the tub curve is one-half of the clock recovery's window requirement in order to maintain a BER of 10^{-10} . If the clock position is not centered in the baud interval, then its true time position must be known in order to determine the actual window time-width for the clock recovery circuit with this technique.

The following specific example shows an estimate for the window time-width of the VSC8117 clock recovery circuit. Refer to Figure 15, Table 3 and Figure 16 for the tub diagram data described below.

Least Squares Fit LOG(-LOG(BER)) vs P_R
1000 m Link, SerDes output

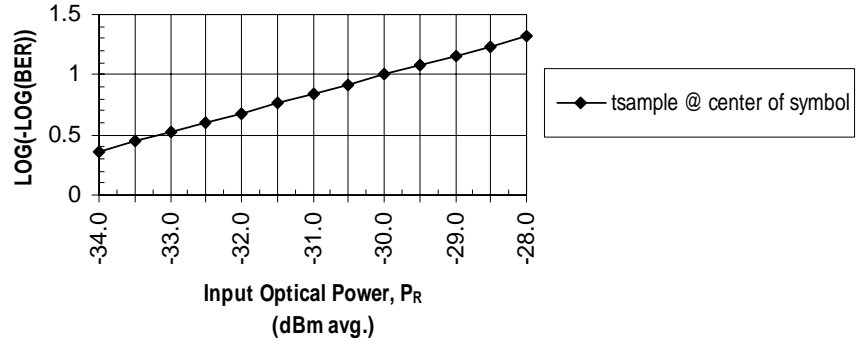


Figure 15. Least Squares Fit of Log (-Log(BER)) vs. Input Optical Power (P_R) for Center of Symbol from SerDes Output with 1000 m 62.5/125 μ m Fiber-Optic Link

Table 3. Conversion Between BER and LOG[-LOG(BER)] Values.

BER	LOG[-LOG(BER)]
10^{-2}	0.3010
10^{-3}	0.4771
10^{-6}	0.7782
10^{-9}	0.9542
10^{-10}	1.0000
10^{-12}	1.0792

P_R vs t_{sampling} at SerDes Input

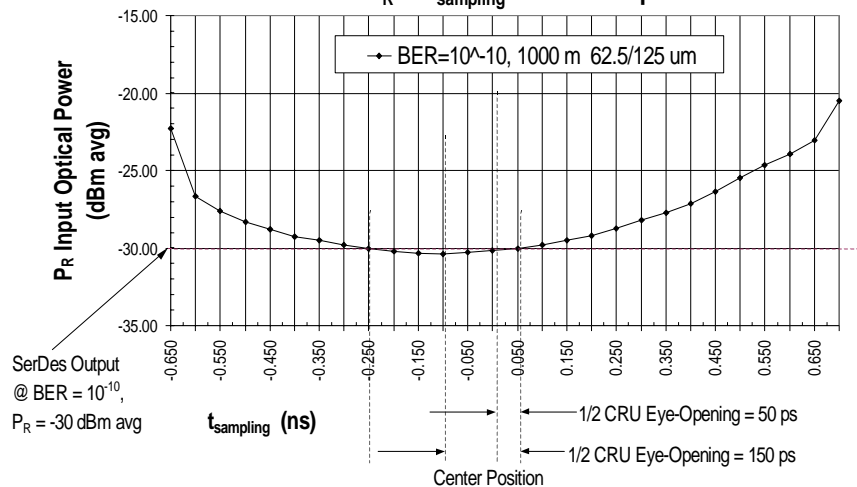


Figure 16. Receiver Input Optical Power (P_R) vs. Clock Sampling Time Position (t_{sampling}) for Constant BER = 10^{-10} for 1000 m Link.

The SerDes's clock recovery window-opening test was done using the 622 MBd reference design circuit. The test conditions were: use of a 1000 meter length of 62.5/125 μm fiber-optic cable, the VSC8117 SerDes is in Facility Loopback mode and the BERT clock is positioned in the center of the retimed serial data output eye-opening. The bit error rate is measured as a function of the fiber-optic receiver sensitivity. The BER values were extrapolated to BER of 10^{-10} and the corresponding input optical power was found to be $P_R = -30$ dBm avg. From the 1000 m/BER = 10^{-10} tub curve, Figure 16, that represents the received data eye-opening to the SerDes's input, and assuming that the SerDes's recovered clock position is at the center of baud interval, the corresponding eye-opening is then twice the 50 ps time interval to the nearest edge (right edge) of the tub curve. The estimated clock recovery window time-width is approximately 100 ps. This is an estimated value because if the SerDes's recovered clock position is to the left of center, then the window time-width would be larger. For example, if the clock position was 100 ps to the left of center, then the window time-width could be approximately 300 ps. If the clock position is any further to the left, the window would become smaller again. Also, at this $P_R = -30$ dBm avg. level, and if the recovered clock position was to the right of center interval by 50 ps, the window time-width becomes essentially zero which is unrealistic. Hence, the most likely estimate for the recovered clock window time-width is between 100 ps to 300 ps. This range of values meets and is within the multimode 622 MBd

ATM-SONET/SDH standard's minimum data eye-opening amount of 310 ps that can be provided to the SerDes for it to meet or exceed the standard's BER of 10^{-10} .

Test Point 3: Fiber-Optic Transmitter Input Data Waveforms

The transmitter input waveforms are of good fidelity, showing minimal reflections. These

waveforms are shown in Figures 17 (Data), 18 (Data-bar) and 19 (Data-Data-bar) for a 500 m length of 62.5/125 μm fiber and with the fiber-optic receiver input optical power adjusted to $P_R = -26.0$ dBm avg. For example, the total Data edge jitter measured at Test Point 3 is 233 ps p-p for ~ 112 k-samples. It is interesting to note that the SerDes's output total Data edge jitter did not change significantly in its peak-to-peak value of

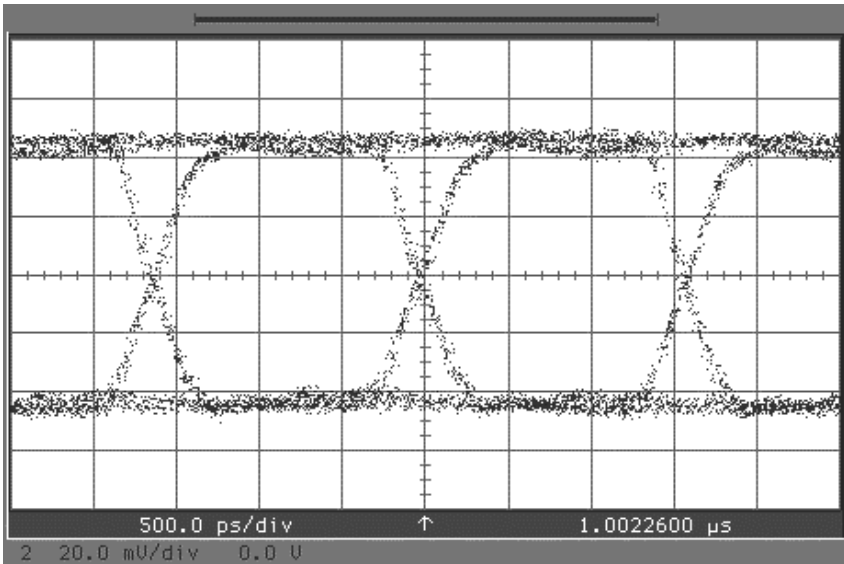


Figure 17. HFBR-5208M Transmitter Serial Data Input with 500 m of 62.5/125 μm fiber and at $P_R = -26$ dBm avg. with the SerDes in Facility Loopback Mode.

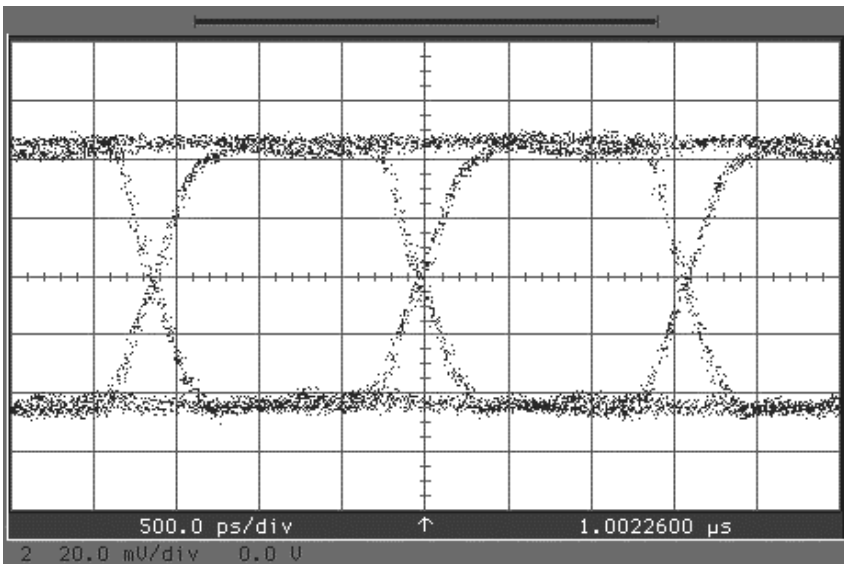


Figure 18. HFBR-5208M Transmitter Serial Data-bar Input with 500 m of 62.5/125 μm fiber and at $P_R = -26$ dBm avg. with the SerDes in Facility Loopback Mode.

approximately 211 ps - 233 ps when either the 1 m, 500 m or 1000 m of multimode fiber was used in the link prior to the SerDes IC. The SerDes was in Facility Loopback mode (serial data loopback). Basically, the SerDes output data jitter was not affected by input signal jitter to the SerDes device. This is due to the good clock recovery/data retiming circuit performance within the SerDes unit and the low-jitter fiber-optic receiver performance.

Test Points 1 to 4: Jitter Tolerance, Jitter Transfer, Jitter Generation Tests

With respect to frequency-based jitter performance, Jitter Tolerance and Jitter Transfer were measured by PMC-Sierra, Inc. for this reference design board using the HFCT-5208M single-mode fiber-optic transceiver. Figure 20 shows the ITU-T SDH 622.08 MBd (STM-4, Type A) Recommendation G.958 actual Jitter Tolerance result compared against the corresponding Mask requirement of that standard. Over the measured jitter frequency range of 200 Hz to 5 MHz, the Jitter Tolerance performance is compliant to the standard's Mask requirement and it has additional margin of performance at all frequency points (above the Mask limit). This measurement was made with the HP 37717C OMNIBER at the minimum input specified receiver sensitivity plus 1 dB (-27 dBm avg.) with a PRBS $2^{23}-1$ data pattern.

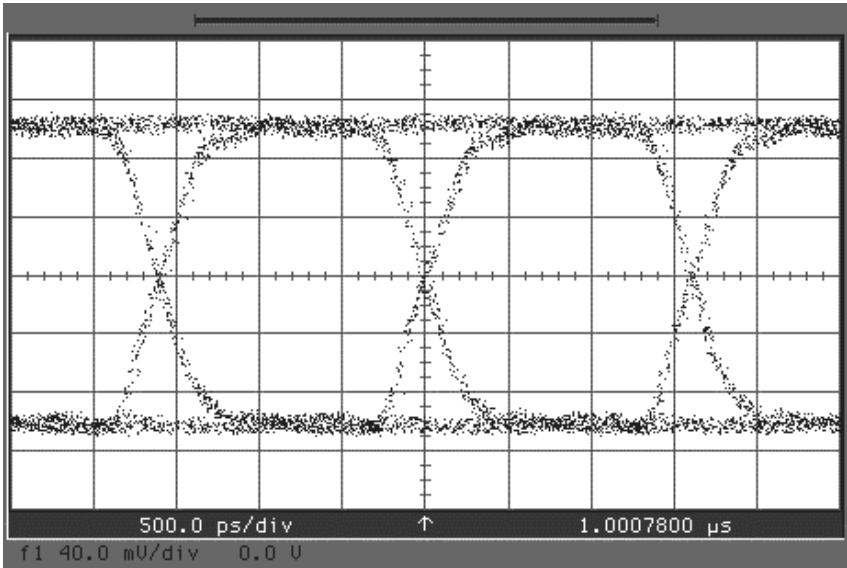


Figure 19. HFBR-5208M Transmitter Serial Differential Data (Data - Data-bar) Input with 500 m of 62.5/125 μm fiber and at $P_R = -26$ dBm avg. with the SerDes in Facility Loopback Mode.

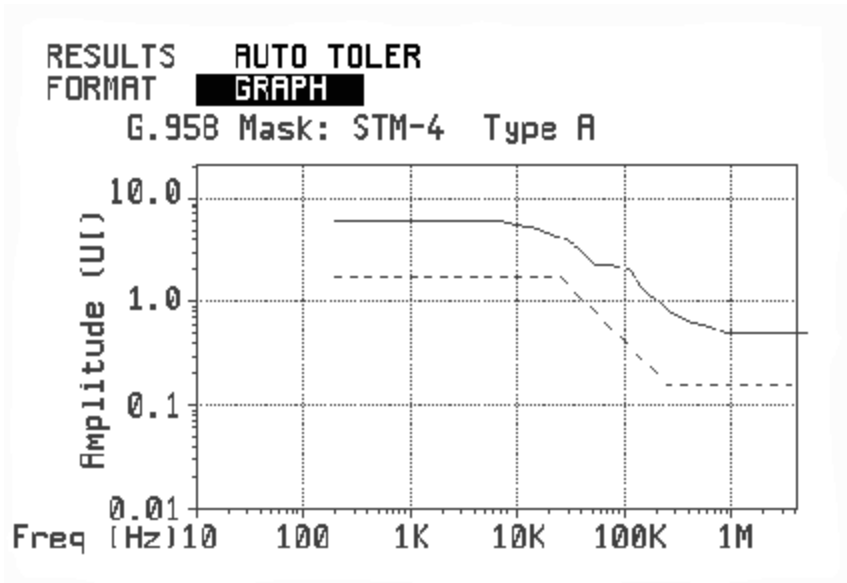


Figure 20. Jitter Tolerance Performance of the 622.08 MBd Reference Design Board per the ITU-T SDH STM-4 Recommendation G.958 Standard.

Similarly, Jitter Transfer was measured for this reference design board with the single-mode fiber-optic transceiver. The circuit was configured in Loop-timed mode. Figures 21 and 22 illustrates the ITU-T SDH 622.08 MBd (STM-4, Type A) Recommendation G.958 actual Jitter Transfer results compared against the corresponding standard's Mask requirement. As can be seen, the Jitter Transfer does not pass this standard's requirement to be within (underneath) the Mask limits. The measured Jitter Transfer -3 dB bandwidth is approximately 5 MHz. Also, Figure 22 shows an enlarged view of Figure 21. As can be seen, there is approximately 0.6 dB of jitter peaking at 1 MHz. In the design of the VSC8117 clock recovery and clock generation PLLs, the Jitter Transfer performance was compromised to improve the upon the Jitter Tolerance performance. Most applications for this VSC8117 will be for non-repeater applications where Jitter Transfer is not of concern. As mentioned earlier in this note, an external, very low bandwidth loop-filter 1x PLL circuit can be used to improve the Jitter Transfer performance. Contact Vitesse Semiconductor's Applications Group for further details about this approach.

Jitter Generation performance for this reference design circuit will be reported when it becomes available from PMC-Sierra, Inc.

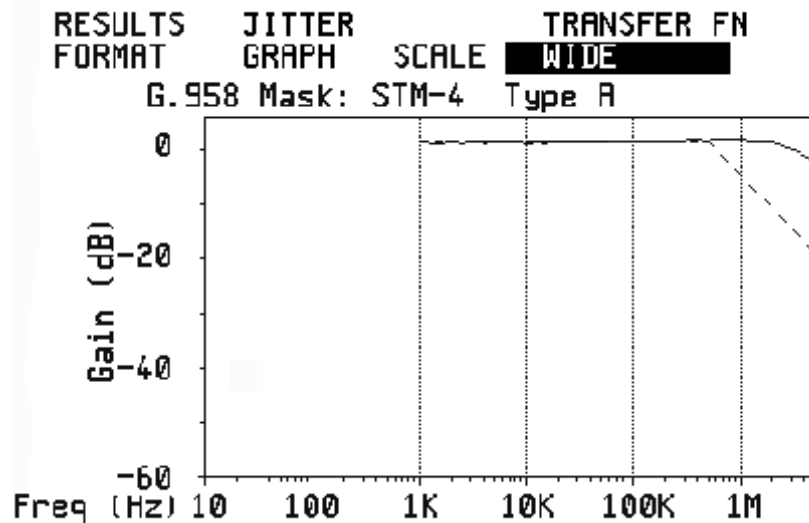


Figure 21. Jitter Transfer Performance of the 622.08 MBd Reference Design Board per the ITU-T SDH STM-4 Recommendation G.958 Standard. Vertical scale is 10 dB per division.

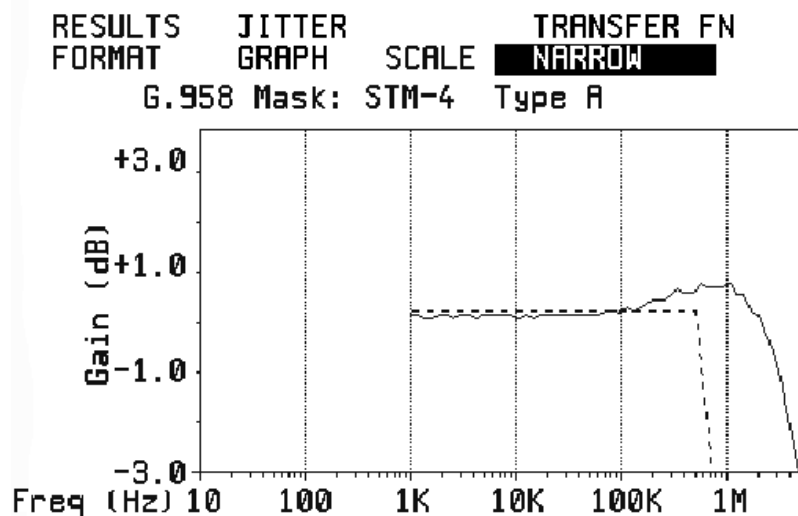


Figure 22. Jitter Transfer Performance of the 622.08 MBd Reference Design Board per the ITU-T SDH STM-4 Recommendation G.958 Standard. Vertical scale is 1 dB per division.

Test Methods

Guidance on Testing Methods

This section explains common techniques used for directly testing and measuring performance of the 622 Mb/sec components on the reference design board.

For testing the reference design board, serial data format is used because common test equipment is available for providing convenient test signals, observing high-speed waveforms and measuring bit-error-ratios. Various fiber cable lengths are tested to show the effects of optical signal dispersion* in a fiber. Note, however, there are many factors that can degrade a signal in a communication link. The purpose of this application note is to explain how to practically measure and quantify these effects as they relate to the 622 Mb/sec standards. This application note does not explain how and why signal degradation occurs since these topics are explained in standard engineering textbooks, articles and literature.

One of the most important parameters that demonstrate how well a serial link is performing is the quality of the data eye-opening. There are related and measurable parameters that quantify the data eye-opening performance for a serial link. They are the time-based jitter of the signal measured by a histogram method. Also, time-based jitter can be observed by measuring the input optical power to the receiver as a function of time position within the data eye-opening for a constant BER condition. As described in detail earlier, this data plotted as a graph is called a "tub" diagram. An eye-mask template measurement of

the transmitter output optical power can be measured as well. Specific data for these types of parameters was shown for various conditions in the section entitled, **Performance Data**.

Explained next is how to measure:

- 1) histogram of time-based data jitter
- 2) a "tub" diagram
- 3) optical eye-mask shape.

Data Jitter Histogram

Measurement of time-based data jitter is done by using a very high-speed sampling oscilloscope, such as the 20 GHz HP83480A with electrical or optical plug-ins, to develop a histogram of the data jitter defined by a proportion of both the signal amplitude and Baud time interval centered at mid-level of the data transition crossings. Some sampling scopes have internal algorithms that automatically measure the data jitter in peak-to-peak or rms values as well as other automatically measured parameters. The trigger for the scope is the highest speed clock that runs the system. The data jitter is not only dependent upon the "threshold window" of voltage and time, but upon the amount of waveform samples taken (or measurement time) and the type of data pattern used for the test.

Measure Receiver Sensitivity vs. t_{sampling} (tub diagram)

Measurement of time-based jitter of the fiber-optic receiver by observing the input optical power (P_R) level needed versus the time position within the output data eye-opening to maintain a constant BER condition ("tub" diagram) is a more involved test. However, this test is very informative and provides an accurate, bit-for-bit error measurement to determine the eye-opening (or total jitter)

over a wide range of P_R levels. The basic measurement technique to create a tub diagram is to sample the returning serial data to the BERT with a BERT clock phase-shifted over the usable data eye-opening without losing synchronization. At each measured time-position, record P_R at BER levels of 10^{-4} , 10^{-5} , 10^{-6} , and 10^{-7} . This BER data is extrapolated by linear regression on a log(-log) scale versus a linear P_R scale which allows a prediction of P_R at the required operating level of BER = 10^{-10} or better. From this graph, the data eye-opening time can be determined at any P_R level of interest.

Measure ATM-SONET/SDH Frequency-based Jitter

Jitter Tolerance, Jitter Transfer, and Jitter Generation test configurations used to measure frequency-based jitter performance of this reference design board will be shown as soon as they become available from PMC-Sierra, Inc. As an example of test settings used with the HP 37717C OMNIBER for Jitter Transfer measurement, they are shown in Figure 23.

* Basically, optical signal dispersion causes the optical signal to spread out over a Baud interval which ultimately will cause more jitter in a link and limit the signaling rate for a given length of fiber cable. Optical dispersion is caused by both modal dispersion (different light modes arrive at different times at the end of the fiber) or chromatic dispersion (different wavelengths arrive at different times at the end of the fiber) in multimode fiber. In single-mode fiber only chromatic dispersion is an issue.

Eye Mask Measurement

Measurement of an eye-mask waveform is straightforward and is done by using the high-speed sampling scope's built-in mask template and an appropriate bandwidth filter for the 622 MBd ATM-SONET/SDH standard. This eye-mask test pertains only to the output optical waveform from the fiber-optic transmitter. The HP83486A 2 GHz 1300 nm single-mode fiber optical-to-electrical plug-in works well for performing

this test. Once the mask is displayed with the use of this plug-in, the built-in eye-mask measurement routine can be automatically run to align the mask to data eye-opening, take samples of the waveforms and log the violations (hits) within the mask and/or the mask's margin areas. This eye-mask test determines whether the optical signal will be of proper shape and eye-opening amount for the subsequent fiber-optic receiver to use.

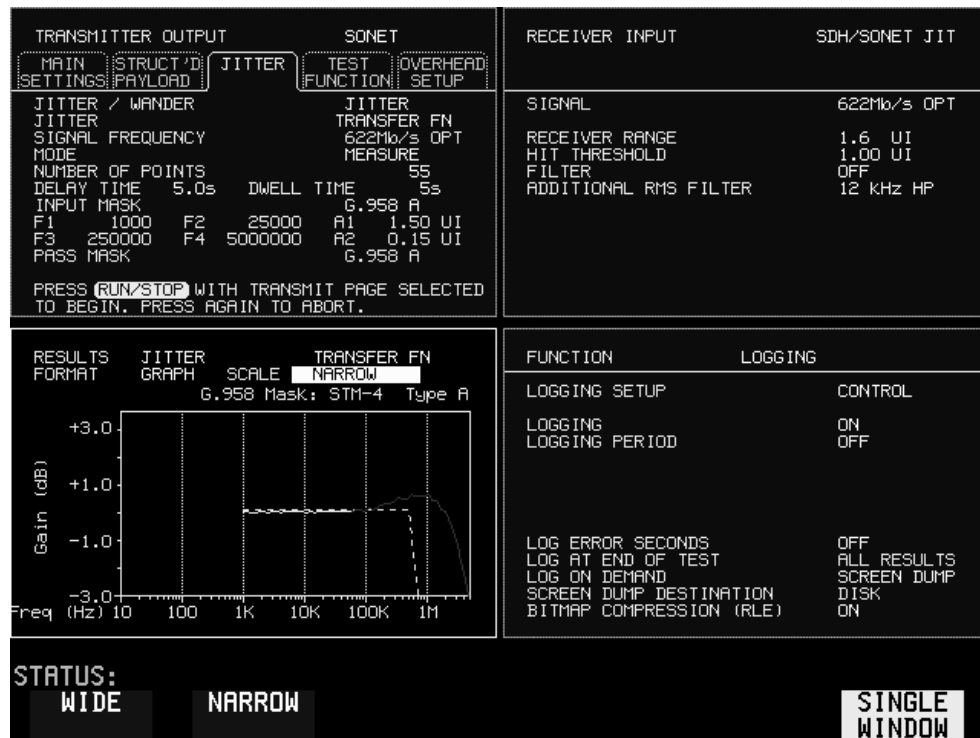


Figure 23. HP 37717C OMNIBER Instrument Test Settings Used to Measure the 622.08 MBd Reference Design Board for Jitter Transfer Performance per the ITU-T SDH STM-4 Recommendation G.958 Standard.

Test Configurations

A recommended test configuration for evaluating the 622 MBd OC-12 fiber-optic transceiver is shown in Figure 24. This test setup uses standard, high-speed test instruments such as a Bit-Error-Ratio Tester (BERT), a sampling oscilloscope and a programmable delay generator. Fiber-optic test equipment needed to measure the optical transceiver performance are a fiber-optic attenuator, optical power meter, an optical-to-electrical converter (O-E), a 70%/30% fiber-optic splitter, fiber-optic

cable and another evaluation board to provide an equivalent BERT signal in optical form. If the 1300 nm LED-based HFBR-5208M transceiver is being tested, then the fiber-optic equipment needs to attenuate, measure and carry 1300 nm light using multimode fiber-optic cable. If the 1300 nm Fabry-Perot Laser-based HFCT-5208M transceiver is being tested, then the fiber-optic equipment needs to attenuate, measure and carry 1300 nm light using single-mode fiber-optic cable.

The recommended sampling oscilloscope, HP83480A, has plug-ins for 1300 nm single-mode fiber (HP83485A) and for 1300 nm multimode fiber (HP83486A). These plug-ins are effectively an O-E converter, an optical power meter and a waveform analyzer combined into one unit. Some general comments about fiber-optic transceiver testing are listed below.

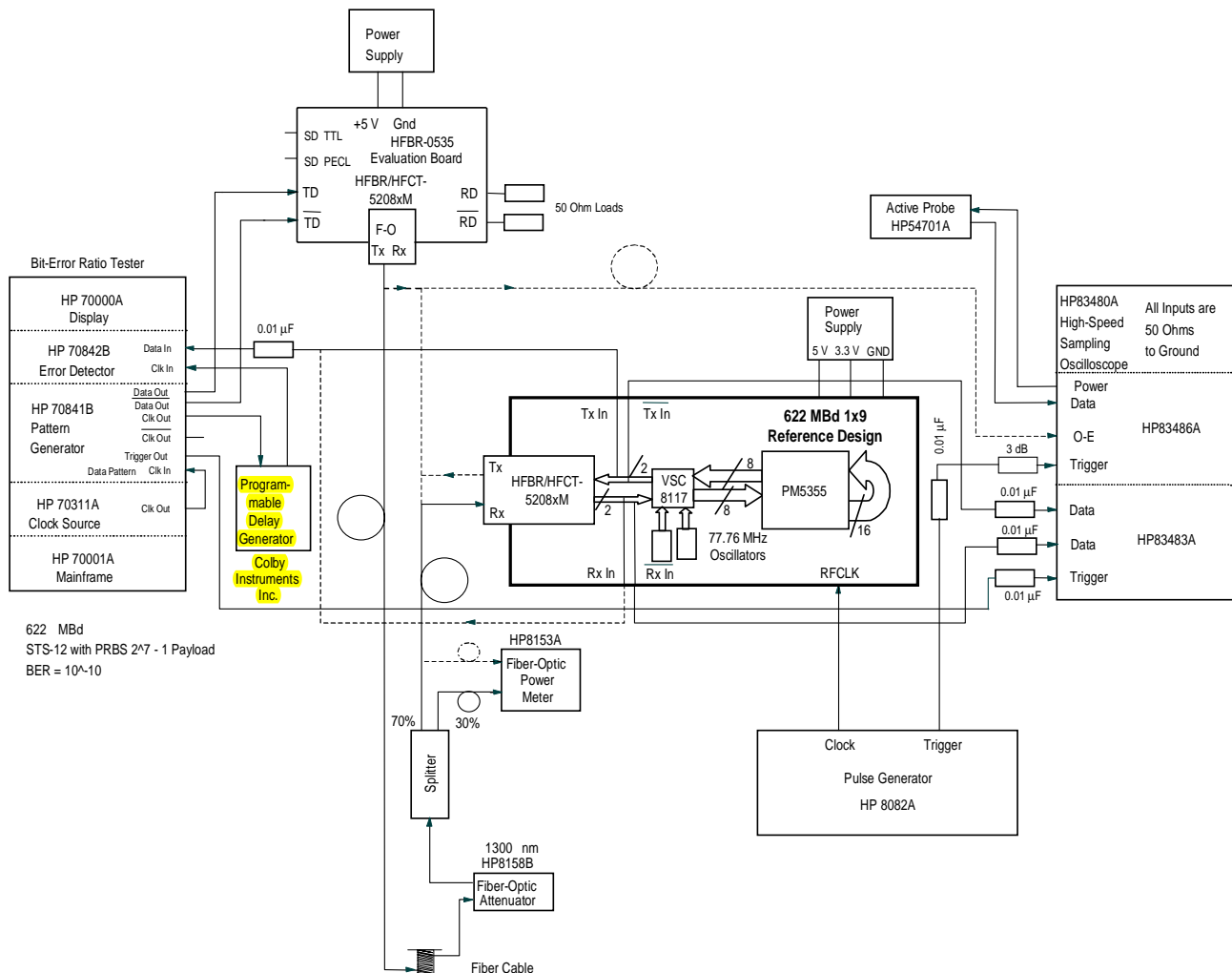


Figure 24. Block Diagram of 622 Mb/sec Test System

Signal Monitoring

Monitoring the active 622 Mb/sec serial data signal between the fiber-optic transceiver and the SerDes unit without affecting the signal is done with an approximate 10:1 voltage divider circuit. This is a convenient method to observe the signal while using high-speed 50 Ohm input test equipment, such as the high-speed HP83480A sampling scope or the HP70000 series BER Tester. Note, when using a high-impedance active probe, instead of the resistive voltage divider circuit, the active probe does not provide as high a measurement bandwidth as does the oscilloscope's 50 Ohm input circuit. In addition, the active probe is sometimes less mechanically convenient to use. The reference design on-board divider is made of a 453 Ohm surface-mount resistor that connects to monitor the signal line. A 50 Ohm transmission line trace connects at one end to this resistor and at the other end of the line connects to a SMA connector that, in turn, connects to 50 Ohm coaxial cable to the 50 Ohm input of the scope. When connecting this resistive divider to the BER Tester serial data input, an in-line 0.01 μF blocking capacitor should be used to remove the small ($\div 10$) dc bias that exists on this line. Both sets of transmit and receive differential data lines have the resistive divider monitoring capability.

A few pitfalls to avoid when testing with this evaluation board and their components are briefly mentioned next.

1. When using the HP70000 series BER Tester with a low-level PECL input signal, such as from the 10:1 resistive divider circuit, the typical minimal signal level the BERT can use is about 60 mV p-p. The 10:1 attenuator circuit provides approximately 80 mV p-p which is adequate to operate the BERT.
2. If an optical power splitter is used with a 622 MBd fiber-optic transmitter in the test setup for measuring a tub diagram, use a 70%/30% optical splitter with low insertion loss to provide a usable optical power range for the fiber-optic receiver.

Test Equipment

Table 4. List of Suggested Test Equipment

Title	Manufacturer	Model Number	Quantity	Notes
Digital Communication Analyzer	Agilent	HP83480A	1	3
Optical/Electrical Module (O-E Plug-in)	Agilent	HP83486A with Optional OC-12 filter	1	1; One channel is for 1300 nm multimode light, one electrical channel is 20 GHz
Optical/Electrical Module (O-E Plug-in)	Agilent	HP83485A	1	1; One channel is for 1300 nm single-mode light, one electrical channel is 20 GHz
Electrical Module (Plug-in)	Agilent	HP83483A	1	Two electrical channels with 20 GHz bandwidth
Active Probe	Agilent	HP54701A	2	10:1 Active Probe has 2.5 GHz bandwidth with 0.6 pF, 100 k Ω input impedance
Bit-Error-Ratio Tester	Agilent	HP70000 Series	1	2
Jitter & Eye-Diagram Analyzer	Agilent or Tektronix	HP71501A Series or Tektronix SJ300	1	Automated measurements of SONET/SDH Jitter Tolerance, Transfer & Generation
Programmable Delay Generator	Colby Instruments, Inc.	CPDL	1	Delay upto 100 ns in 10 ps steps
Pulse Generator	Agilent	HP8082A	1	Use an equivalent Instrument to this if unavailable (obsolete)
Optical Power Meter	Agilent	HP8153A	1	Use with two HP81533A plug-in modules
Optical Power Heads	Agilent	HP81521B	2	Optical Heads necessary for HP8153A meter
Optical Attenuator	Agilent or JDS	HP8158B option 002 & 011 or JDS HA9	1	For multimode & single-mode fibers
Optical Splitter	Canstar (or equivalent)	MR4-B-62.5 10676	1	70%/30% split ratio for 62.5/125 μ m fiber
Fiber-Optic Cables	Siecor; Red Hawk	Siecor TB-1KM-62-ST-SM (1 km); Red Hawk CD-97245-02 (500m);	1	62.5/125 μ m multimode fiber
Power Supplies	Agilent	HP6236B; HP E3601A	1	Triple Output, 6 V dc/2.5 A, \pm 20 V dc/0.5 A; Single Output, 8 V dc/ 3 A or 15 V dc/2 A
622.08 Mb/s Reference Design Board	Agilent	Version 1.1	1	Test Circuit
1x9 Evaluation Board	Agilent	HFBR-0535	1	Provides electrical to optical conversion
Multimode and Single-mode 1 x 9 Fiber-optic Transceivers	Agilent	HFBR-5208xM HFCT-5208xM	2	Multimode Single-mode
Miscellaneous Wire and Fiber-optic Accessories	Agilent; Picosecond Pulse Labs; Fiber-optic connector suppliers: Amphenol, Red Hawk, Siecor	HP11742A 0.01 μ F; PPLabs 5501A, 5502A 0.01 μ F; HP8493A -3 dB, HP8493C -20 dB attenuators	Varies	SMA Coupling Capacitors, Attenuators, Terminations, SMA-connector Coaxial Cables; Fiber-optic connector adapters

Notes:

1. Optical-to-Electrical

Converter: The optical 622 MBd LED- or Laser-based transmitter performance was measured with an optical-to-electrical converter designed for 1300 nm operation with approximately 2 GHz bandwidth. The optical transmitter signal dynamic performance can be measured against the transmitter eye-mask template. With this O-E converter plug-in for the HP83480A oscilloscope, the optical extinction ratio, rise/fall times, pulse-width distortion and jitter can be measured.

2. **BERT:** For receiver sensitivity test at the center of the data eye-opening, the BERT can automatically self-align and sample the receiver output data at the center of the baud interval. For receiver sensitivity at the left or right of the center baud time position, then a programmable delay generator must delay the sampling clock edge to the appropriate time position within the eye-opening.

3. HP83480A High-speed

Sampling Scope: Measure extinction ratio automatically with this scope. Basically, the transmitter extinction ratio is equal to $[P_{on}/P_{off}]100\%$ in percent or as $10\log[P_{on}/P_{off}]$ in dB. A mask template can be custom configured or a pre-configured internal mask can be used. For convenience, an internal SONET/SDH OC-12 mask can be used for 622.08 MBd testing. The HP83480A 20 GHz scope can save data to memory for later non-real-time analysis or for storage to floppy disk file for documentation needs.

Conclusions

As seen from the information presented in this application note, the designer can quickly use this proven, three-vendor developed, standards'-compliant reference design to create a 622.08 Mb/s, OC-12 ATM-SONET/SDH Physical Layer interface with Framers function. With a common electrical and mechanical interface for the fiber-optic multimode and single-mode units, design changes to the circuit are minimal or not required when interchanging fiber-optic interfaces. This gives flexibility to the design without modifying the SerDes and Framers circuitry.

In addition, the quantified data that was measured and shown about this reference design helps support the designer in the effort to achieve a working design on the first attempt. Test methods and configurations were given to help designers understand how best to check performance of their design. Also, guidance was provided to assist the designer in printed circuit board layout, in circuit designing with the SerDes or the Framers ICs and the fiber-optic transceivers. Unique information about the operation of these devices was discussed in this note.

Armed with this application note's guidance, a designer can quickly and successfully develop a flexible 622 Mb/s OC-12 ATM-SONET/SDH Physical Layer interface with minimal time, resource and expense.

Appendix

Contents: **Bill of Materials**
Design Rules - PCB Transmission Lines & Construction
Reference Information

Bill of Materials: **Table A1. HFBR/HFCT-5208M Reference Design Board Bill of Materials.**

Designator	Amt	Part Type	Size	Part Number	Vendor
R1, R2, R3, R4, R5, R6, R7, R151	8	270 Ω \pm 5%, 0.1 W	0603	CR0603-10W271JT	Venkel
R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R148, R149, R150	31	33 Ω \pm 5%, 0.1 W	0603	CR0603-10W330JT	Venkel
R39, R52, R119	3	75 Ω \pm 5%, 0.1 W	0603	CR0603-10W750JT	Venkel
R42, R43, R44, R45, R46, R47, R48, R49, R50, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R117, R142, R143, R144,	57	1 k Ω \pm 5%, 0.1 W	0603	CR0603-10W102JT	Venkel
[R51, R72, R73, R153, R154]	[5]	[1 k Ω \pm 5%, 0.1 W]	[0603]	[CR0603-10W102JT]	[Venkel No Load]
R99, R101, R102, R103, R104, R105, R106, R107, R108, R109, R110, R111, R112, R113, R136, R137, R140	17	0 Ω +0.05 Ω max., 0.1 W	0603	CR0603-10W0R0JT	Venkel
R114, R115, R116, R118	4	10 k Ω \pm 5%, 0.1 W	0603	CR0603-10W103JT	Venkel
[R120, R138]	[2]	[82 Ω \pm 5%, 0.1 W]	[0603]	[CR0603-10W820JT]	[Venkel No Load]
[R121, R139]	[2]	[130 Ω \pm 5%, 0.1 W]	[0603]	[CR0603-10W131JT]	[Venkel No Load]
R122, R124, R125	3	100 Ω \pm 5%, 0.1 W	0603	CR0603-10W101JT	Venkel
R123	1	510 Ω \pm 5%, 0.1 W	0603	CR0603-10W511JT	Venkel
R126	1	470 Ω \pm 5%, 0.1 W	0603	CR0603-10W471JT	Venkel
R127, R128, R129, R130	4	453 Ω \pm 1%, 0.1 W	0603	CR0603-10W4530FT	Venkel

Bill of Materials: Table A1. (continued)

Designator	Amt	Part Type	Size	Part Number	Vendor
R131, R132	2	120 Ω \pm 5%, 0.1 W	0603	CR0603-10W121JT	Venkel
R133, R134	2	160 Ω \pm 5%, 0.1 W	0603	CR0603-10W161JT	Venkel
R135	1	220 Ω \pm 5%, 0.1 W	0603	CR0603-10W221JT	Venkel
[R145, R146, R155, R156]	[4]	[0 Ω +0.05W max., 0.1 W]	[0603]	[CR0603-10W0R0JT]	[Venkel No Load]
[R147]	[1]	[390 Ω \pm 5%, 0.1 W]	[0603]	[CR0603-10W391JT]	[Venkel No Load]
R152	1	51 Ω \pm 5%, 0.5 W	1210	CR1210-2W510JT	Venkel
C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C15, C16, C18, C19, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C61, C62, C64, C66, C76, C80, C81	44	0.1 μ F \pm 10%, 25 V dc, X7R	0805	C0805X7R250104KNB	Venkel
C44, C45	2	1.0 μ F \pm 20%, 25 V dc, Tantalum	B	TA025TCM105MBN	Venkel
C46, C74, C75	3	33 μ F \pm 20%, 16 V dc, Tantalum	C	TA016TCM336MCN	Venkel
C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60	14	10 μ F \pm 20%, 16 V dc, Tantalum	B	TA016TCM106MBN	Venkel
C68, C69, C70, C71, C72, C73, C79, C82, C83	9	0.01 μ F \pm 10%, 16 V dc, X7R	0603	C0603X7R160103KNB	Venkel
[C77, C78]	[2]	[0.1 μ F \pm 10%, 16 V dc, X7R]	[0603]	[C0603X7R160104KNB]	[Venkel No Load]
L1, L2	2	10 μ H \pm 5%, 150 mA	1260	NL322522T-100J-3 or equivalent	TDK
L3, L4, L5, L6	4	1.0 μ H \pm 5%, 400 mA	1260	NL322522T-1R0J-3 or equivalent	TDK
D1, D2, D3, D4, D6	5	Surface-Mount Red LED	1206	HSMH-C650	Agilent
D5	1	Surface-Mount Green LED,	1206	HSMG-C650	Agilent
U1	1	622/155 Mb/s ATM/SONET/SDH Serializer/Deserializer with Clock Recovery and Clock Generation	64 lead PQFP	VSC8117	Vitesse Semiconductor Corp.
U2	1	622 MBd ATM-SONET/SDH Framer	208 lead PQFP	PM5355	PMC-Sierra, Inc.

Bill of Materials: Table A1. (continued)

Designator	Amt	Part Type	Size	Part Number	Vendor
U3	1	Dual PECL-to-TTL Translator	SO-8	MC100ELT23	Motorola
U4	1	Multimode/Single-Mode Fiber-Optic Transceiver	1 x 9	HFBR/HFCT-5208M	Agilent
U5	1	77.76 MHz 5 V dc PECL 3 rd Overtone Crystal Oscillator	4 pin (14)DIP or 4-lead SMT or 6-lead SMT	VF161SH-C- 77.76 MHz, SEL3411AA-77.7600 MHz VF561SH-77.76 MHz SEL3601B-77.7600 MHz	Valpey-Fisher, Saronix Valpey-Fisher Saronix
U6	1	77.76 MHz 5 V dc AC MOS TTL Crystal Oscillator	4 pin (14)DIP or 4-lead SMT	VFAC170 - 77.76 MHz, STA090C-77.7600 MHz VFAC570-77.76 MHz STA09FC-77.7600 MHz	Valpey-Fisher, Saronix Valpey-Fisher, Saronix
U7	1	Quiet Series Quad 2-Input NAND Gate	SO-14	74ACTQ00	Fairchild Semiconductor Corp.
S1	1	8-Gang SPST Switch	DIP-16	CTS 208-8	CTS Corp.
J2, J3, J4, J5, J6, J27, J28, J33, J34, J35	10	2-pin Header and Associated Jumper (only 4 jumpers are used with these 10 headers)	DIP-2	4-103186-0 (80 pin DIP Header) 65474-004 (Jumper)	AMP Inc.
J13, J14, J23, J24, J25, J26, J31, J32, J36, J37, J38	11	SMA Vertical Mount Connector	SMA	142-0701-201	E F Johnson
J100	1	Power Connection Header and Connector	1 row x 6 pins	641208-6 (Header) 641217-6 (Connector)	AMP Inc.
	17	Single-pin Socket	0.038" OD x 0.136"L	6-330808-5	AMP Inc.
	4	Standoff with Internal Thread	0.75", 6-32	0380-0091	Lyn-Tron Inc.
	4	Machine Screws	0.438", 6-32	6C43PPMS	The Olander Company, Inc.
	1	Printed Circuit Board	4.8" x 5.8"	622 MBd 1 x 9 Reference Design, Agilent/Vitesse/PMC-Sierra, Version 1.1	Agilent

[] represents component normally not loaded onto reference design board.

Design Rules for Printed Circuit Transmission Lines

The high speed serial data lines that connect the SerDes IC to the 622 MBd module should be constructed as either stripline or microstrip transmission lines. For this reference design board the transmission lines were constructed as microstrip lines. Figure A1 defines the dimensions for a stripline transmission line. In this case the signal trace is sandwiched in the dielectric material of the printed circuit board (PCB) equidistant from the two conducting ground planes. Impedance of the stripline is determined by the relative dielectric constant of the PCB material (ϵ_r), the thickness of the dielectric (b), the width of the transmission line (w), and the thickness (t) of the copper trace.

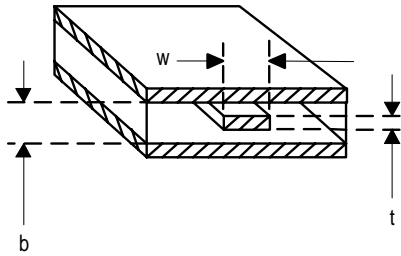


Figure A1 Stripline Transmission Line

The characteristic impedance of the stripline can be calculated using Equation 1.

Equation 1

$$Z_o = \frac{60}{\sqrt{\epsilon_r}} \ln \left[\frac{4b}{0.67\pi(0.8w+t)} \right]$$

Additional stripline transmission line parameters of interest are delay time per unit length and capacitance per unit length.

Equation 2

$$t_{pd} = 1.017\sqrt{\epsilon_r} \quad (\text{ns/ft})$$

Equation 3

$$C_o = \frac{t_{pd}}{Z_o} \quad (\text{pF/ft})$$

Figure A2 defines the dimensions for a microstrip transmission line. In this case the transmission line is open to the air on the top or bottom layer of the printed circuit board, and ground or power planes are located on the inner layers of the printed circuit. The impedance of the microstrip line is determined by the relative dielectric constant of the PCB material (ϵ_r), the thickness of the dielectric (h), the width of the transmission line (w), and the thickness (t) of the copper trace.

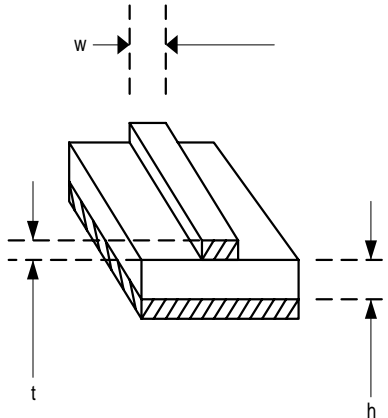


Figure A2 Microstrip Transmission Line

The characteristic impedance of the microstrip transmission line can be calculated using Equation 4.

Equation 4

$$Z_o = \frac{87}{\sqrt{\epsilon_r + 1.41}} \ln \left[\frac{5.98h}{0.8w + t} \right]$$

In this reference design, version 1.1, the 50 Ohm and 75 Ohm microstrip transmission lines were made with trace widths of 0.012 in (0.305 mm) and 0.005 in (0.127 mm) respectively.

Additional microstrip transmission line parameters of interest are delay time per unit length and capacitance per unit length. The given formulas below provide the specific values for this reference design board.

Equation 5

$$t_{pd} = 1.017\sqrt{0.475\epsilon_r + 0.67} \quad (\text{ns/ft})$$

For $\epsilon_r = 4.63$, $t_{pd} = 128$ ps/in

Equation 6

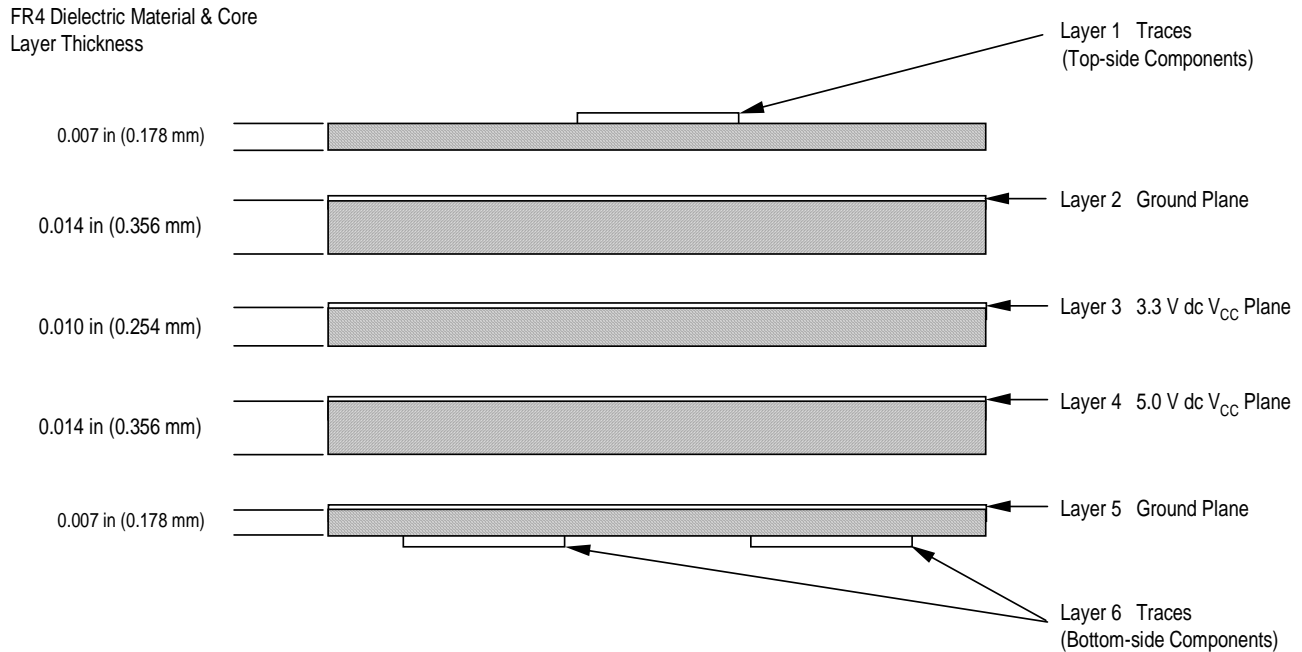
$$C_o = \frac{t_{pd}}{Z_o} \quad (\text{pF/ft})$$

For $Z_o = 50$ Ohm line, $C_o = 2.56$ pF/in

For $Z_o = 75$ Ohm line, $C_o = 1.71$ pF/in

Printed Circuit Board Construction

The 622 MBd reference design board (version 1.1) in Figure 5 is made using microstrip transmission lines on layers 1 and 6. No stripline transmission lines were used within this board. The board is constructed with FR4 material and is of 0.062 in (1.57 mm) total thickness with six-layer printed circuit board structure as shown in Figure A3 below.



Layers 1 and 6 are 1¼ oz. Copper Foil and ½ oz. Plating. Total Thickness = 0.0023 in (0.0584 mm)

Layers 2, 3, 4 and 5 are 1 oz Copper Foil. Thickness = 0.0013 in (0.0330 mm)

FR4 Relative Dielectric Constant = 4.63

Figure A3. Printed Circuit Board Construction for 622 MBd Reference Design Board

Reference Information

For more information and technical support on Agilent fiber-optic components, the following contact points are available.

Web Site: www.agilent.com
Corporate-wide information, including components
www.semiconductor.agilent.com
Fiber-optic component information

Component Customer Response Center: 1.800.235.0312

Component Fax-back Service: 1.800.450.9455

Component Field Sales Engineer:
Contact local Agilent Sales Office

Component Field Applications Engineer:
Contact local Agilent Sales Office

Component Factory Applications Engineer:
Contact local Agilent Sales Office

High-Speed Design

Johnson, Howard W. & Martin Graham, *High-Speed Digital Design A Handbook of Black Magic*, Prentice Hall PTR, Englewood Cliffs, New Jersey, 1993.

Blood, Jr., William R., *MECL System Design Handbook*, Fourth Edition, Motorola Semiconductor Products Inc., 1988.

Wadell, Brian C., *Transmission Line Design Handbook*, Teradyne, Inc., Artech House, Inc., Norwood, Massachusetts, 1991.

Layout Practices

Montrose, Mark I., *Printed Circuit Board Design Techniques for EMC Compliance*, IEEE PRESS, Piscataway, New Jersey, 1996.

Testing Methods

Derickson, Dennis, *Fiber Optic Test and Measurement*, Hewlett-Packard Company, Prentice Hall PTR, Upper Saddle River, New Jersey, 1998.

EMI Prevention

Application Note 1166, Minimizing Radiated Emissions of High-Speed Data Communications Systems, Agilent Technologies, 5968-4810E, March 1999.

Williams, Tim, *EMC for Product Designers*, Second Edition, Newnes, Butterworth-Heinemann, Oxford, England, 1996.

Ott, Henry W., *Noise Reduction in Electronic Systems*, John Wiley, New York, New York, 1988.



Standards Documents

American National Standards Institute Inc. (ANSI) T1.646-1995 Broadband ISDN – Physical Layer Specification for User-Network Interfaces Including DS1/ATM

T1.646a-1997 Supplement to ANSI T1.646-1995

ANSI T1.416.01-1998 and T1.416.02-1998 Network to Customer Installation Interfaces – Synchronous Optical NETWORK (SONET) Physical Media Dependent Specification: Multi-Mode Fiber and Single-Mode Fiber (respectively)

ANSI T1.105.06-199x Synchronous Optical Network (SONET): Physical Layer Specifications

The ATM Forum Technical Committee 622.08 Mbps Physical Layer Specification af-phy-0046.000 January 1996

ITU-T Recommendation G.957 Optical Interfaces for Equipments and Systems Relating to the Synchronous Digital Hierarchy, 1990

ITU-Recommendation G.958 Digital Line Systems Based On The Synchronous Digital Hierarchy For Use On Optical Fibre Cables, 1990

Eye Safety Information

Application Note 1109, LED Eye Safety, Agilent Technologies, 5965-7734, May 1997.

Supportive Web Sites

www.agilent.com
Agilent Technologies, Corporate-wide information, including components

www.semiconductor.agilent.com
Agilent Technologies, Fiber-optic component information

www.tm.agilent.com/tmo/TMTop/English
Agilent Technologies, Test and Measurement Organization

www.vitesse.com
Vitesse Semiconductor Corporation

www.pmc-sierra.com
PMC-Sierra, Incorporated

www.signalintegrity.com
High-Speed Digital Design, Web Site of Dr. Howard Johnson of Olympic Technology Group, Inc., Redmond, Washington, 1999.

Data Sheets

HFBR-5208M Family, 1300 nm LED, HFCT-5208M Family, 1300 nm FP Laser, 1 x 9 Fiber Optic Transceivers for 622 Mb/s ATM/SONET/SDH Applications, Agilent Technologies, August 1999.

VSC8117 ATM/SONET/SDH 622/155 Mb/s Transceiver Mux/Demux with Integrated Clock Generation and Clock Recovery®, Vitesse Semiconductor Corporation, Camarillo, California, 1999.

PM5355 S/UNI-622™ Saturn User Network Interface (622-Mbit/s) Standard Product. PMC-Sierra, Inc., PMC-941027 Issue 3, Burnaby, British Columbia, Canada, June 1998.

www.semiconductor.agilent.com

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