

Dewar-to-Dewar Data Transfer at 2 Gigabits per Second

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Abstract—Digital circuits have been developed to interface superconductive electronic chips with high speed 50- Ω transmission lines. Digital data at 2 Gigabits per second was transferred from a Josephson chip in a first cryostat to another Josephson chip in a second cryostat. The chips were connected by more than 3 meters of 50- Ω transmission line. No semiconductor amplifiers were used in this data path. A Hewlett Packard data source provided the original data to the first chip, which converted it to SFQ data. Output interface circuits were driven by a 2-GHz external clock to latch series strings of 10 junctions and drive 2-Gbps data into a 50- Ω cable. In the second cryostat, a latching three-junction interferometer with a two-turn control line converted the input signal to latched data and switched an MVTL OR-gate output. This demonstration showed that low-power Josephson digital circuits can be integrated into multichip digital subsystems that can pass data at high rates without the use of power-hungry semiconductor amplifiers.

I. INTRODUCTION

To exploit the speed advantage of Josephson digital electronics, chip to chip data transfer at GHz rates is required. Digital systems rarely succeed in putting all functions on a single chip. The successive generations of personal computers illustrate how the number of chips stays the same, despite higher integration levels. To succeed, superconductive electronics needs to develop methods to transfer data between superconductive chips and from superconductive to semiconductor digital chips at high speeds.

Commercial and military communication systems face growing demands for high speed data links. The very high speed and low power of superconductive electronics (SCE) technology can meet this need in a much more compact footprint than can conventional technology, enabling near-GHz data rates with high security, jamming immunity, fade resistance, and covertness. These desirable performance features are achieved with a direct-sequence spread-spectrum modulator-demodulator (modem), supporting multiple

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simultaneous links using code-division-multiple-access (CDMA) protocols [1]. Northrop Grumman and Lincoln Lab are collaborating to develop a superconductive modem.

The modem uses two superconductive chips. Northrop Grumman is developing a code generator that uses single-flux-quantum (SFQ) logic [2]; while Lincoln Laboratory is developing a programmable binary/analog matched filter for data detection and demodulation using analog and latching-logic components [3]. Implementation of the spread-spectrum modem will require communication between superconductive chips as well as between those chips and ambient-temperature electronics outside the cryogenic enclosure. The demonstration reported here addressed both those needs by exercising the driver and receiver circuits that will be used for off-chip and inter-chip communication.

Signal levels in SCE chips—especially in SFQ logic chips—are very low compared to those in semiconductor circuits. The Northrop Grumman test chip used in this demonstration contains an SFQ generator and an amplifier circuit that converts the small SFQ pulses into signals that can drive a 50- Ω cable out of its cryostat. The Lincoln test chip used in the demonstration contains a receiver circuit that can detect the incoming signal while maintaining immunity to spurious signals resulting from pickup loops between the cryostats and voltage bounce on the chip's ground plane. The chip also contains the first gate of a shift register.

This paper describes a demonstration in which a superconductive digital chip in one dewar drove 2 gigabit per second (Gbps) data through 50- Ω cable to another superconductive digital chip in a different dewar. No semiconductor amplifiers were used in this critical data path.

This paper also describes an improved 10X latching amplifier. It was faster, produced a higher output voltage, and had a lower bit error rate, 10^{-7} at 2 GHz.

II. JOSEPHSON CHIPS

The experiment used two chips in two different dewars. The first dewar contained a chip fabricated at Northrop Grumman. Fig. 1 shows the functional blocks which converted input data to SFQ data. The output interface used three stages of latching amplifier - 1X, 3X, and 10X [4].

The second dewar contained a chip fabricated at Lincoln Lab. Its functional blocks are shown in Fig. 2. The input was a 3-Junction Logic latch [5], in which the control line was wrapped twice over the latching SQUID to reduce the trigger threshold for the input DATA current. The output

MVTL gate [6] is the same type used in the programmable matched filter [3].

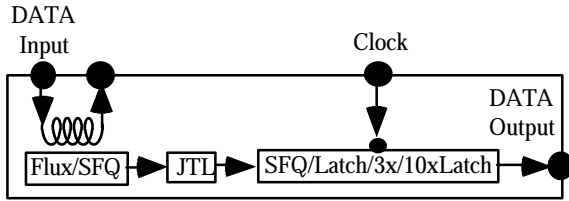


Fig. 1. Chip fabricated at Northrop Grumman. Semiconductor data current was inductively coupled to an SFQ generator and launched SFQ pulses into a Josephson transmission line in the asynchronous part of this chip. Stored flux was clocked into a latch, which triggered a 3X latch, which triggered a 10X output latch.

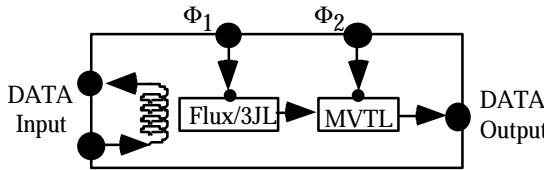


Fig. 2. Chip fabricated at Lincoln Lab. Data currents were inductively coupled into a 3-Junction Logic input gate on clock phase_1, which triggered the output MVTL gate on clock phase_2.

III. DATA TRANSFER BETWEEN DEWARS

The block diagram in Fig. 3 shows the arrangement of the apparatus used for the demonstration. Both SCE chips were clocked at 2 GHz using a signal derived from an HP frequency synthesizer that served as the master reference. The Northrop Grumman chip used several dc biases plus a single, sine-wave clock derived by attenuating and level-shifting the reference sine wave. This clock signal was also sent to the Tektronix sampling scope for display. The Lincoln chip, although it can operate using sine-wave clocks, was clocked with fast-rise-time square-wave clocks in order to subject its input to greater stress by introducing larger switching transients in the ground plane.

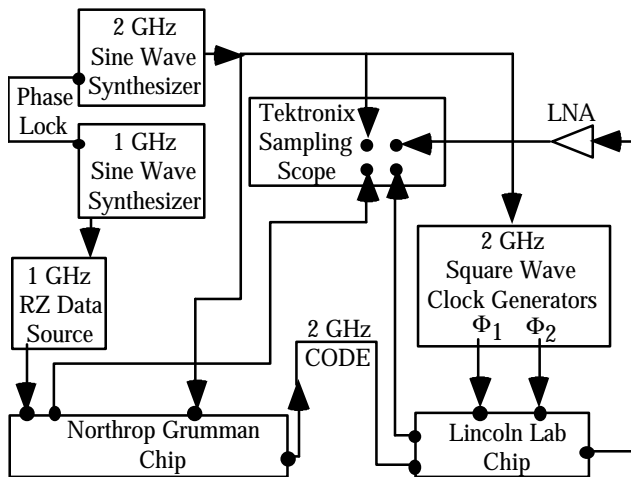


Fig. 3. Block diagram of the demonstration of data transfer at 2 Gbps. Both chips were driven by 2 GHz clocks. The fastest that the semiconductor source

could generate Return to Zero data was 1 Gbps, so half of the data bits were “0.”

The Northrop Grumman test chip requires a return-to-zero (RZ) input data pattern. This was provided by the word generator, which could be clocked at a maximum frequency of 1 GHz. Its input clock was derived in effect by dividing the master clock source by two. The output from the word generator was sent to the input of the Northrop Grumman chip.

The output from the Northrop Grumman chip was then sent to the Lincoln chip, whose input is inductively coupled and floating with respect to its chip-ground. The signal enters via one pin and is returned for external termination via another pin. The return signal was sent to the Tektronix scope, which allowed it to be viewed while providing the required termination. The output from the logic gate in the Lincoln chip was sent through a wide-band, low-noise amplifier to the sampling scope. To avoid ground pickup loops, high speed lines were ac-coupled to 50-Ω terminations [4].

Fig. 4 shows the apparatus. Two liquid-helium cryostats can be seen in the foreground, each containing a high-speed test probe. The one on the left contained the Northrop Grumman chip; the one on the right contained the Lincoln Laboratory chip. The cable labeled “2 GHz CODE” carried the signal left-to-right from one cryostat to the other. The instrument in the upper left corner is the HP model 8660C Synthesized Signal Generator that provided the 2-GHz master clock. The identical synthesizer below it was set to a frequency of 1 GHz and phase locked to the upper synthesizer. Its output was used to clock the HP 80000 Data Generator System at the far right side of the picture. The output data pattern can be seen on its display.

To the right of the frequency synthesizers on the shelf is the Tektronix model 11801 Digital Sampling Oscilloscope. The lower instrument to the right of the scope is a Colby Instruments model 5000A pulse generator capable of generating a pair of clocks at up to 5 GHz with rise times of about 50 ps. It provided the clocks used by the Lincoln chip. The three instruments at the right edge of the shelf are Colby Instruments model 10A and 30A digitally controlled precision delay lines. They were used to set the relative phases of the various clock signals.

A printout of the scope display is shown in Fig. 5. The top trace is the 2-GHz clock applied to the Northrop Grumman chip. The second trace is the output from the HP word generator. The data represent the 15-chip pseudo-noise sequence {111011001010000} that the Northrop Grumman prototype code generator chip provides. Because the word generator can make RZ data only up to 1 GHz, the actual data effectively have “0” bits between each of the code bits thereby forming the 30-bit 2-GHz sequence {101010001010000010001000000000}. The Flux-to-SFQ converter on the Northrop Grumman chip responds to this signal.

The third trace shows the signal from the output driver of the Northrop Grumman chip after it has passed through the input coupler in the receiver on the Lincoln chip. The delay of approximately 12 ns results from the additional cable length to the scope. The bottom trace shows the output



Fig. 4. Josephson digital circuits in separate cryostats transferred data through more than 3 meters of cable at 2 Gbps without using semiconductor amplifiers.

signal from the final logic gate on the Lincoln chip after it has been amplified by a room-temperature semiconductor amplifier. The further delay of about 10 ns again results from the extra cable length in the path.

5 nsec/division; relative delays between traces are not significant, due to unequal cable lengths.

IV. IMPROVED 10X LATCH

A new 10X latch has been developed to overcome problems with the old design [4]. The latch used in the demonstration of dewar-to-dewar data transfer was designed to drive 15 to 20 mV into a 50-Ω cable. In tests, it produced these levels at 200 MHz, but at 2 GHz, the data rate for the superconductive modem, it output only about 8 mV. There was also a reset problem, false “1s” following true data “1s”.

To obtain faster operation, the improved 10X latch was designed to trigger directly from a 1X latch, without the 3X stage. Also, the string of 25 unshunted JJs, used to control ground ripple currents on the high-speed output, was eliminated. To reduce reset errors, more damping was used on the first latching junction of the input string. Finally, new software was used for parameter extraction from mask

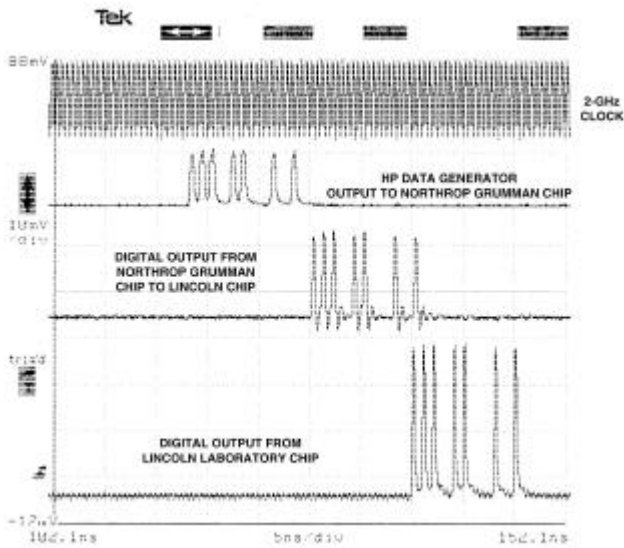


Fig. 5. Screen print from the sampling scope shows the 2-GHz Clock (top trace), the original 2 Gbps data after passing from the Data Source through the first Josephson chip to the scope (first data trace), the output of the 10X latch in the first cryostat after passing unamplified through the second Josephson chip (middle data trace at 2 mV/division), and the amplified output data from the second Josephson chip in the second cryostat (bottom data trace). Time scale is

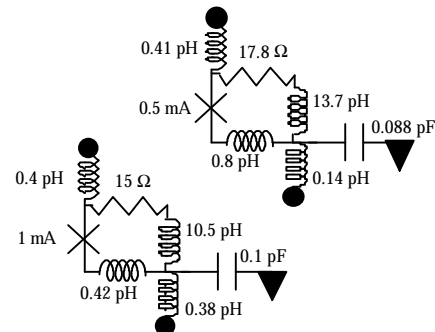


Fig. 6. Parameter extraction from mask layouts was combined with simulation optimization to yield these values for shunted junctions used in the improved 10X latch. The 0.5-mA junctions used 17.8-ohm shunts and the 1-mA junctions used 15-ohm shunts.

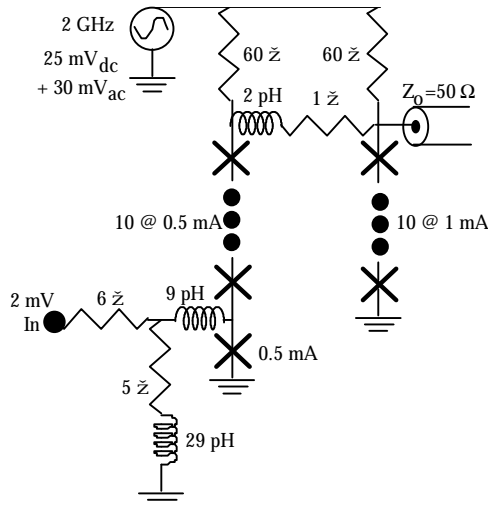


Fig. 7. The improved 10X latch used series strings of the shunted junctions from Fig. 6. It was triggered by a 1X latch input, had a low Bit Error Rate of 10^{-7} at 2 GHz, and operated up to 5 GHz.

layout. Fig 6 shows how the parasitic inductances and capacitance were included in the circuit optimization.

The new 10X latch was constructed from 11 junctions on the input side and 10 junctions on the output side, as shown in Fig. 7.

The improved 10X latch was tested with pseudorandom data input at 2 Gbps and produced a 15-mV output. The mask test feature of the sampling scope was used to test for both the false “1” reset error and the false “0” failure to latch [4]. At optimal bias the bit error rate (BER) was 10^{-7} at 2 Gbps. The BER increased at higher operating speeds, but the 10X latch was still useful up to 5 GHz for demonstrating operation of SFQ circuits.

V. DISCUSSION

We have demonstrated that 2 Gbps data can be transferred between superconductive digital chips through more than 3 meters of 50- Ω cable, without using any semiconductor amplifiers in this critical data path. The 10X latching amplifier drove sufficient signal power into the cable to permit detection by a SCE chip in another cryostat.

The superconductive spread spectrum modem can tolerate relatively high bit error rates in this data path, because the matched filter compares all of the received chips to all of the code chips. At 15 or 63 chips per data bit, one or two errors in transferring the code chips will not significantly degrade the correlation. So a BER less than 10^{-3} is sufficient.

For other parts of the modem and for other applications requiring data transfer with lower BER, more power is desired in the data signal. The improved 10X latch produced more output power by turning on faster, increasing the duty cycle and achieving a peak output voltage of 15 mV. Even larger output signals were developed by Suzuki, who used series strings of more than 50 latching junctions to develop a 100-mV output signal at 1 GHz [7]. However, long strings switch more slowly than short strings, so we developed 10X latches for multi-Gbps data transfer [8].

The receiver circuit on the Lincoln Lab chip detected the

data, even though the 10X latch used in the demonstration did not produce its full design voltage. The intrinsic thermal noise current in a Josephson junction is of the order of $5 \mu\text{A}_{\text{rms}}$. For a BER of 10^{-16} , the signal power should be 20 dB larger than the noise power. From Fig. 5, the data signal was about $70 \mu\text{A}_{\text{pp}}$ when it reached the scope and, estimating cable losses, about $100 \mu\text{A}_{\text{pp}}$ when it reached the Lincoln Lab chip. Clearly, more signal power is desired to allow margins for cable losses, interference and other noise currents.

Future efforts may achieve more improvement by matching the impedance of the SCE output driver to the 50- Ω output line, than by attempting to increase output voltage. A single, 2-mA output junction with a 1- Ω damping resistor dumps 50X more power into its shunt than it drives into the 50- Ω output line. Impedance matching could harness an additional 17 dB of output power, enabling reliable data communication between SCE and room temperature circuits at tens of GHz.

The results reported here have clearly demonstrated that circuits have been developed to enable a spread spectrum code generator to transmit code to a programmable matched filter chip through meters of 50- Ω cable at data rates of 2 Gbps. This demonstration showed that low-power Josephson digital circuits can be integrated into multichip digital subsystems that can pass data at high rates without the use of power-hungry semiconductor amplifiers.

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