OPTICAL NETWORK INTERFACE DESIGN
ONIDS
SYMPOSIUM

PAPER 5

622 MBd ATM/SONET/SDH PHY Reference Design Development

By Dick Jamison

Abstract

Design issues, test techniques and the resulting measured data from a standards-compliant 622 MBd reference design used in OC-12 ATM/SONET/SDH applications are examined in this paper. This design provides a common interface circuit and footprint for either a multimode (MMF) or a single-mode (SMF) fiber optic application by using HP's interchangeable HFBR-5208 (multimode) or HFCT-5208 (single-mode) 1x 9 pinout fiber optic transceivers. The fiber optic transceivers are used with Vitesse Semiconductor VSC8117, a serializer/deserializer/clock recovery/clock generation integrated circuit (IC) along with the PMC-Sierra PM5355 framer and ATM cell processor IC. The design development and the results presented in this paper provide the designer with a proven, standards-compliant three IC solution for 622 MBd OC-12 ATM/SONET/SDH physical layer designs.

Biography

Richard E. Jamison
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Mr. Jamison has 24 years of engineering design experience in analog, digital, and optical subsystems. During the past 20 years at HP, he has been involved in product characterization, measurements and applications of optoelectronic products for communication, particularly optocouplers and fiber optic components. He is an Applications Engineer for the Optical Communication Division of HP and has authored several articles and application notes for its product lines. In the past few years, Dick has supported divisions products in applications for FDDI, ATM, and other fiber optic network standards. He has a BSEE from the University of Massachusetts (Amherst) in 1966, and from Boston College a MS in Teaching Physics (1975) and Masters in Physics (1978).

Introduction

This paper provides design guidance, test techniques, performance data and suggested layout recommendations for a 622 MBd ATM/SONET/SDH physical layer interface reference circuit. This standards-compliant reference design provides a convenient, interchangeable MMF or SMF fiber optic interface via a common interface circuit and component footprint. The fiber optic transceivers used in this reference design are 1 x 9 pinout MMF HFBR-5208 and single-mode SMF devices. The fiber optic transceivers are used with a Vitesse Semiconductor VSC8117 serializer/deserializer/clock recovery/clock generation integrated circuit (SerDes IC) along with a PMC-Sierra PM5355 framer and ATM cell processor IC. Using the presented information, designers will be able to directly copy the necessary portion of the circuit and layout for use on a printed circuit board to save product development time, resources and expense. Overall, this reference design is compliant with the ANSI T1.646/T1.646a 622 MBd ATM/SONET/SDH standard for multimode and single-mode applications.

As results in the *Performance Data* section of this paper show, this reference design's compliance with ATM standards requirements serve the product developer well. The design's good performance is demonstrated through a low bit error rate, the need for only a small clock recovery window opening, excellent fiber optic receiver sensitivity, extra margin for the single-mode, optical eye-mask, and good frequency-based jitter performance for the single-mode, fiber optic transceiver and clock recovery/generation circuitry, etc. The reader should review the *Performance Data* section for details.

The main topics discussed in this paper include:

- Circuit Interfaces
- SerDes Comments
- Framer Comments
- PCB Layout
- Performance Data
- Test Methods
- Conclusion

Circuit Interfaces

Reference Design Basic Function

The basic reference design's circuit is of a loop-back configuration. A high-speed, serial 622 MBd optical signal is sent to the circuit board where it is converted into high-speed serial data and clock signals. In turn, the signals are converted to 8-bit parallel data by the SerDes IC. The 8-bit data is then passed onto the framer IC and processed. The framer output 16-bit bus is looped-back into the framer, this data is passed back to the 8-bit bus for reserializing, and retiming of the data by an on-board clock generator in the SerDes. The reserialized data is then sent off-board as a serial 622 MBd optical signal.

For various test configurations, this reference design circuit is very flexible. For example, the serial data can be looped-back at the input to the deserializer to analyze just the serial portion of the circuit. This is called the Facility Loopback Mode of the SerDes IC. Control signals for the serializer/deserializer can be set to specific conditions to allow various modes of operation or diagnosis. Alternate reference clock inputs can be used for improving low-frequency jitter performance of the SerDes transmit phase-locked loop. Figure 1 illustrates a block diagram of the 622 MBd reference design. It depicts only the essential interconnections for the circuit. Figure 2 shows a photograph of the 622 MBd reference design board.

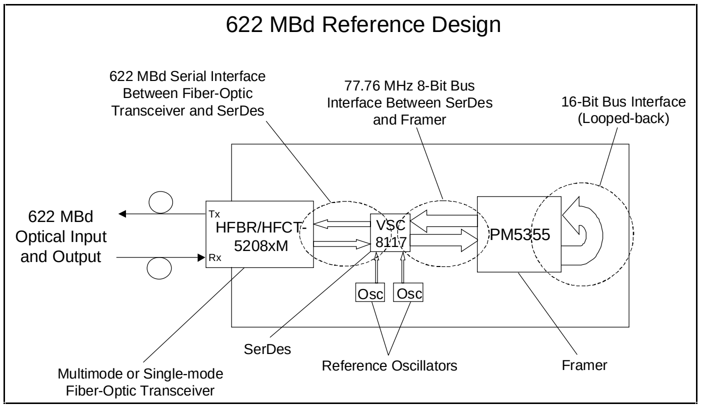


Figure 5-1 622 MBd Reference Design Block Diagram

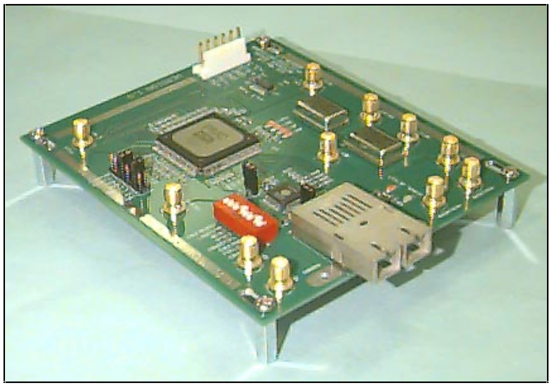


Figure 5-2 622 MBd Reference Design Photograph

Serial Interface: Fiber Optic Transceiver and SerDes IC

The high-speed serial interface between the fiber optic transceiver and the SerDes device is relatively simple and straight-forward to design. This section only describes the circuit interface design issues. High-speed signal fidelity concerns and board layout issues will be discussed in the *PCB Layout* section. Figure 3 shows the simplified interface circuit to use for networking equipment. Refer to HP application note, AN 1178 for complete detailed information on design and testing options.

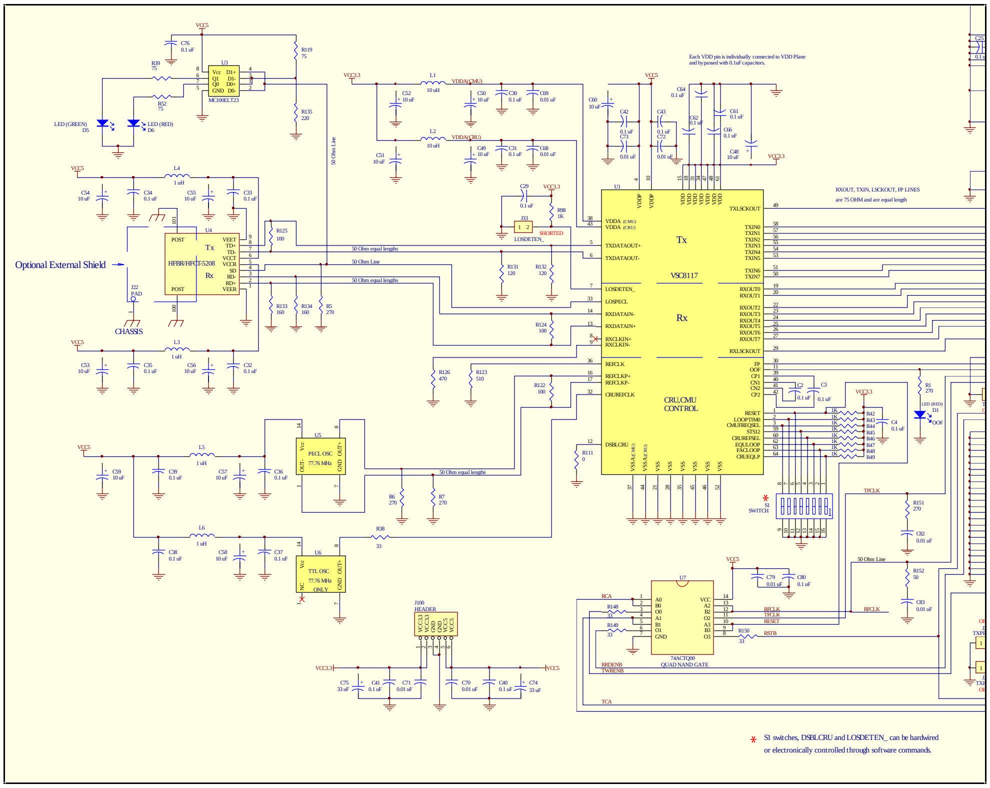


Figure 5-3 Simplified 622 MBd Interface Circuit Between Fiber Optic Transceiver and SerDes IC

As shown in Figure 3, the 5 Vdc PECL 622 MBd serial data lines to and from the fiber optic transceiver are directly connected to the SerDes input and output via 50 Ohm differential transmission lines. At the fiber optic receiver source end of the lines, each output has a biasing resistor of 160 Ohms to ground. This 160 Ohm value provides a low impedance path that quickly pulls-down the emitter follower output. This helps the output fall time be more symmetric with the output rise time to reduce common-mode EMI generation. At the load end of the fiber optic receiver data transmission lines, there is a 100 Ohm line-to-line resistor that terminates the data at the SerDes input. Similarly, the SerDes data output has source biasing pull down resistors of 120 Ohms that send PECL signals via 50 Ohm differential transmission lines to the fiber optic transmitter input stage where another 100 Ohm line-to-line resistor terminates the lines.

The Signal Detect (SD) is connected directly to the SerDes's LOSPECL input via a 50 Ohm transmission line. A 270 Ohm pull-down resistor is needed only at the fiber optic receiver SD output. Since this line infrequently switches state, power consumption can be saved by not terminating this line in the standard 50 Ohm PECL manner. Even though there is an alternate Loss of Signal circuit provided by the VSC8117 which can be used if the fiber optic receiver data outputs go to static state levels when the input optical signal is removed, this is not the case with the HFBR/HFCT-5208 transceivers. The receivers will output PECL-level noise chatter, not static data state levels. When the PECL Signal Detect output is permanently connected to the SerDes, the alternate LOS circuit is defeated. More information about this alternate LOS circuit will be mentioned in the *SerDes Comments* section. A 5 Vdc PECL-to-TTL translation circuit (MC100ELT23) is provided to light green or red LEDs to indicate whether SD is asserted or de-asserted (receiving or not receiving useable signal) respectively. Typical HFBR-5208M SD de-assert level is approximately –33.4 dBm average and asserts at approximately at –30.6 dBm average, yielding a hysteresis amount of 2.8 dB. The corresponding de-assert BER level is in the range of 10^{-3} – 10^{-4}.

The power supply filter circuit for the HFBR/HFCT-5208 is the same for both multimode and single-mode transceivers. There are two identical, but separate, V_{CC} filter circuits used; one circuit for the transmitter section and one for the receiver section. The inductor-capacitor (LC) filter circuits provide good power supply noise rejection from the board and reduce crosstalk as well. The filter components should be located as close as possible to the respective V_{CC} power pins. The recommended inductors are TDK Corporation 1 µH surface-mount inductors with part number NL322522T-1R0J-3 or equivalent. The 0.01 µF capacitors on the V_{CC} pin side of the filter should be adjacent to the pin. All 0.01 µF capacitors should be high-quality, monolithic ceramic bypass capacitors.

Parallel Interface: SerDes and Framer

There are two 8-bit bus circuits and two corresponding byte clock circuits for interfacing between the VSC8117 SerDes and the PM5355 Framer ICs as shown in Figure 3. The reference design board's transmit data (TXIN) and receive data (RXOUT) 8-bit bus interfaces are slightly simplified for use in a regular application circuit. The simplification removes jumpers in the TXLSCLKOUT and RXLSCLKOUT lines as well as removes 0 Ohm resistors in the RXOUT lines. The 0 Ohm resistors were place-holder resistors for use in dampening potential ringing on the lines. The individual RXOUT and 8-bit byte clock (RXLSCKOUT) lines should be 75 Ohms or higher impedance because the output driver stages do not properly support lower impedance lines. Each RXOUT line should be of equal length. The RXLSCKOUT line length should also equal the RXOUT line length. This minimizes bit skewing on the bus.

The line length is equally important for the TXIN data and TXLSCKOUT byte clock lines. However, the corresponding POUT line drivers of the PM5355 are capable of driving 50 Ohm lines. Since the TXLSCKOUT driver needs a 75 Ohm line, it is recommended that all 8-bit bus and clock lines be the same 75 Ohm impedance to minimize bus timing skew. The line lengths for the TXIN/TXLSCKOUT lines do not need to equal the RXOUT/RXLSCKOUT lines in length; they only need to match line lengths within each bus.

The interconnecting Frame Pulse signal path from VSC8117 to PM5355 should have the same line length and impedance as the RXOUT/RXLSCKOUT lines. It is a good practice to use 33 Ohm resistors in the TXIN (POUT) lines next to the respective outputs since the lines are driven by CMOS drivers that switch approximately 5 V signals in a short transition time that can cause ringing on the lines.

The 3.3 Vdc TTL RXOUT/RXLSCKOUT signals are of sufficient signal swing to adequately drive the CMOS TTL PIN 8-bit data bus inputs of the PM5355. Conversely, the VSC8117's TXIN input 8-bit data bus lines are designed to accept the CMOS 5 Vdc POUT signals from the PM5355 even though the VSC8117 is powered by 3.3 Vdc V_{CC}. In the reference design circuit, there are SMA connection points to access the TXLSCKOUT and RXLSCKOUT signals. See further details about special use of RXLSCKOUT signal in the *SerDes Comments* section.

Proper V_{DD} filtering of the SerDes device protects the unit from having marginal or unacceptable data error performance. The V_{DD} power supply pins are bypassed with X7R surface-mount 0.1 µF capacitors. Of the seven V_{DD} power pins, two neighboring pins share a bypass capacitor. The overall V_{DD} is bypassed by a 10 µF capacitor for additional low-frequency V_{DD} noise attenuation. Also, the two V_{DDP} PECL power supply pins are treated in similar fashion as the V_{DD} power pins.

The two V_{DDA} analog power supply pins for the Clock Recovery Unit (CRU) and Clock Multiplier Unit (CMU) Phase Locked Loop circuits are individually filtered for extra V_{DDA} noise rejection. This helps minimize any noise that may add unwanted jitter to the PLL performance. The surface-mount inductor-capacitor filter circuit (LC) provides a low-bandwidth V_{DDA} filter that arrests noise frequencies over a broad frequency range. The two filter circuits are not just bypassing, but actually filtering the V_{DDA} pins.

All bypassing and filtering circuits should be located as close as possible to their respective power pins for best noise reduction effects. Note that use of a ferrite bead in place of the surface-mount coil inductor in the LC filter will not provide as effective a low-frequency V_{DDA} noise filter circuit as does the coil inductor circuit. The weak-rejection frequency point for the coil inductor LC filter circuit is at its fundamental resonance frequency of approximately 15.8 kHz where the noise rejection is non-existent, and the resonant contributes to make the V_{DDA} noise worst. Otherwise, the LC filter attenuates at twice the rate that a RC bypassing circuit would do.

SerDes Comments

Different topics of interest about the VSC8117 SerDes application in this design are outlined in this section. The comments will help designers understand some unique design issues and how best to use the VSC8117 part.

To minimize noise coupling into the two analog circuit PLLs within the SerDes IC, the 0.1 µF PLL loop filter capacitors (C2, C3) need to be located very close to their respective pins on the VSC8117. Excess inductance or noise coupling on the nodes will result in additional jitter on the recovered clock or the transmit clock. This additional jitter would lead to sub-optimal bit error performance on the received data or poor jitter generation performance for the transmitted data.

The reference oscillator for use with the SerDes IC needs to be carefully selected. For the Clock Multiplier Unit's (CMU) reference oscillator, a crystal oscillator with ±20 ppm stability needs to be used for public network ATM/SONET/SDH applications. Avoid PLL-based oscillators for this stability requirement.

It is possible to use either a 77.76 MHz or a 19.44 MHz reference crystal oscillator with the VSC8117 on this reference design by changing the appropriate DIP switch settings. It is better to use a higher frequency crystal oscillator for the reference oscillator because there are more transitions from the oscillator to help keep the PLL on frequency. Use a 77.76 MHz crystal oscillator instead of a 19.44 MHz crystal oscillator for standard 622.08 MBd application. In this reference design, a 5 V differential PECL, 3rd overtone crystal oscillator was chosen over a single-ended TTL oscillator for better frequency stability performance. As for the Clock Recovery Unit's (CRU) reference oscillator, a simple ACMOS/TTL crystal oscillator works fine since the oscillator is only keeping the CRU operating near the recovered clock's frequency of 622 MHz.

The dual-in-line, 8-gang slide switches (S1) are set to the normal control and operating positions for a standard 622 MBd application.

In this application circuit, the switch labeled “FACLOOP” is a convenient switch for allowing the data from the fiber optic transceiver output to be serially looped-back at the input clock recovery/data re-timing circuit of the VSC8117 unit back to the fiber optic transceiver input (“OFF” position). When the FACLOOP switch is in the “ON” position for normal application circuit use, the serial data from the fiber optic transceiver is sent onward to be de-serialized, and then past on to the framer IC. For a complete functional description of the switches, refer to the Vitesse Semiconductor VSC8117 data sheet.

The VSC8117 IC has a Loss of Signal (LOS) detection circuit that can be used to:

- Monitor serial data activity
- Determine if data activity has ceased for a determined period of time (no transitions for more than 128 bits)
- Indicate a LOS existence
- Flag the framer IC of LOS state by causing the 8-bit bus to go to an all-zeros condition.

This LOS feature can be used if the Signal Detect (SD) signal from the fiber optic receiver is not connected at the VSC8117 LOSPECL input and the fiber optic receiver data lines can become inactive for a sufficient length of time. In normal applications with the components, the SD signal is used and not the LOS circuit.

The VSC8117’s RXLSCKOUT 8-bit byte clock can be used as a 77.76 MHz clock source for an external, very low loop-bandwidth 77.76 MHz PLL circuit, that can be used to improve jitter transfer performance of the VSC8117. Also for convenience, the TXLSCKOUT 8-bit byte clock is available for a trigger or a transmit byte-clock monitoring point.

Since there is no external clock recovery circuit used in this application, the VSC8117 RXCLKIN- and DSBLCRU are grounded. An optional REFCLK (TTL) input is available for use as the reference oscillator input for the VSC8117 Clock Multiplier Unit in the event the PECL REFCLKP± oscillator is not used. This REFCLK input is accessible via the REFCLK SMA connector on the reference design board.

Dual Rate Applications (155 MBd/622 MBd)

Some designers would be interested in using this reference design circuit for a dual data rate application, either 155.52 Mb/s (OC-3) or 622.08 Mb/s (OC-12). Although the HFBR/HFCT-5208M, VSC8117, and PM5355 can operate at either data rate, performance of the HFBR/HFCT-5208M is only guaranteed at 622 Mb/s. Additionally, the PM5355 requires a microprocessor controller to operate at other than 622.08 MB/s.

Framer Comments

Avoid clock-to-bus or line-to-line skew on bus connections. The data and byte clock lines should be matched in length and in impedance value. For example, the setup and hold times for the 16-bit bus data lines must be satisfied to allow the bus signals to be properly clocked into the PM5355. In the reference design circuit, the 16-bit bus is looped-back with bus lines of equal length and equal impedance. The TFCLK (byte clock) meets the required setup and hold timing for this clock input relative to the bus data lines.

The 16-bit bus is clocked out of the PM5355 by RFCLK and the 16-bit bus is clocked into the PM5355 by TFCLK. The clocks need to operate fast enough to prevent the respective input and output registers from overflowing. Both of the clock signals must not operate beyond 52 MHz. On the reference design board are two options for supplying the clocks:

1. The RFCLK and TFCLK signals can be provided independently via two, separate SMA clock inputs.
2. An external RFCLK signal is supplied to the RFCLK SMA connector. An on-board inverter option is used to create TFCLK. The set-up and hold times of the 16-bit data bus input (TDAT#) are met with the rising edge of TFCLK. This TFCLK rising edge occurs after RFCLK rising edge by the combined half period of RFCLK, plus the propagation delay of the inverter device and the delay of the printed circuit board trace.

There are eight header pins on the reference design board for the PM5355; six are for monitoring signals and two are for jumper connections of this IC. The monitoring header pins must not be jumpered (shorted) together. The pins are TXPRTY0, TXPRTY1, TSOC, GROCLK, GTOCLK, and FPOUT. The two jumper connections are RSOC and TLAIS. Consult the PMC-Sierra PM5355 data sheet for specifics.

Four red LEDs are operated by the PM5355 on the reference design board. Two LEDs monitor the status of the SONET/SDH framing. The LEDs are labeled Loss of Frame (LOF) and Out of Frame (OOF). When the PM5355 is provided a valid SONET/SDH frame the LEDs will be off. If the frames are not correct or missing, the LEDs will be turned on. There is a Loss of Signal (LOS) LED that is turned on when the PM5355 determines that a valid loss of incoming signal has occurred (20 µs ±3 µs of consecutive all-zeros condition on the 8-bit bus input). Also, the LAIS LED will light when an alarm (111 pattern is detected in bits 6, 7, and 8 of the K2 byte for 3 or 5 consecutive frames) is inserted into the data.

As mentioned in the *SerDes Comments* section, the 8-bit bus interface between the SerDes to the PM5355 framer (3.3 V TTL to 5 V TTL) has sufficient 3.3 V TTL signal swing to operate the 5 V TTL input properly. Also, from the PM5355 framer to the SerDes (5 V TTL to 3.3 V TTL), the SerDes's 3.3 V TTL input is 5 V TTL tolerant. In addition, the 5 V TTL 16-bit and 8-bit bus signals from the CMOS PM5355 framer outputs use a 33 Ohm resistor to help reduce ringing on the lines due to the fast 5 V logic transitions.

For more in-depth information about the PM5355 framer IC, consult its complete data sheet at PMC-Sierra's web site: www.pmc-sierra.com.

General Guidance

The following information for PCB layout is listed in the following topic sections. The reference design circuit board followed the recommendations and achieved a working board from the first layout. Additional details on the reference design board layout and construction is given in the HP application note AN 1178 *Appendix*.

Signal Fidelity

1. Position the fiber optic transceiver and SerDes devices reasonably close together for the 622 Mb/s high-speed serial data lines, an inch (25 mm) or so is reasonable. Use either microstrip or stripline techniques to create differential 50 Ohm characteristic impedance transmission lines for the data paths. Regardless of how short the data paths may be, always design them as transmission lines of low characteristic impedance to help control parasitic effects that adversely affect circuit performance.
2. Keep the differential transmission lines of equal length to minimize pulse-width distortion and time skew. Route the lines together to avoid unequal crosstalk coupling. Avoid 90° bends in the transmission line traces. Instead, use uniform radius curves or 45° bends to minimize impedance discontinuities on the lines. Avoid unbalanced or single ended use of differential lines to prevent introducing unwanted pulse-width distortion.
3. Terminate transmission lines properly with a load impedance equal to the characteristic impedance of the line at the end of the line where the signal is to be used by the input of the follow-on device. This helps minimize reflections (ringing). Less ringing keeps the data eye opening wide and contributes to less EMI emissions. Keep biasing resistors on the output of the fiber optic transceiver and the output of the SerDes unit close to the source end of their lines.
4. Should differently powered PECL logic be interfaced, for example, 5 V PECL interfacing with 3.3 V PECL, then ac-coupling capacitors are used in the high-speed, serial data lines. Place the capacitors and any vias in the lines at the source end or at the load end of the transmission line; do not place either of the items in the middle of the lines. Use surface-mount components, typically of 0603 package size, to minimize parasitic effects from influencing the circuits.
5. Use of continuous power and ground planes is essential for best noise performance. Generally, avoid gaps, or special cuts, in the ground planes unless specifically recommended by a component supplier. Ground each VSS, VEE component pin individually to its respective ground plane; do not daisy-chain the ground pins together and then ground the combination of pins at one point.

   Avoid use of sockets for 622 Mb/s signals, unless the sockets are necessary for testing or evaluation purposes. Sockets were used on this reference design board to allow interchanging fiber optic transceivers as well as reference frequency crystal oscillators. Multi-layer boards are a necessity for signal interconnections.

6. Place component power pin bypass capacitors carefully. First, and best to do if possible, a 0.1 µF or 0.01 µF bypass capacitor should be placed directly across the VCC (or VDD) leads and its neighboring ground leads. This bypass capacitor location is on the same side of the board where the component leads are located. The bypass capacitor location is then nearest to the leads, and any traces and vias that are used to connect to the respective V_{CC} or ground planes must connect after the capacitor. If this placement is not possible, then the bypass capacitor should be a 0.1 µF capacitance value and not a 0.01 µF value. The larger bypass capacitor value helps prevent the added trace and via inductance from canceling a significant portion of the 0.01 µF bypass capacitance.
7. To avoid timing skew effects when the parallel bus traces are interconnected between the SerDes and framer ICs or between the framer IC and an upper level IC, the individual data and associated byte clock lines must be close to the same lengths as possible to avoid timing skew effects. Length and impedance of data and byte-clock lines may be limited because of either setup and hold time constraints at a bus input, or limited by the output stage to drive a line adequately. On the reference design board the 8-bit and 16-bit bus data and byte-clock lines were matched in length and impedance as best as possible.
8. Refer to analog 3.3 Vdc V_{DDA} power supply of the VSC8117 SerDes unit, a small island in the 3.3 Vdc power plane was made to separate the digitally noisy 3.3 Vdc power plane from this LC-filtered V_{DDA} connection for the on-board clock recovery and clock generation PLL circuits. This analog 3.3 Vdc island is quite small in size and does not interfere with the main 3.3 Vdc power plane.

Mechanical Aspects

External EMI metal shields are available for the fiber optic products based on this design. Consult the HFBR/HFCT-5208M data sheet and HP application note AN 1178 for more information.

Artwork, Gerber Files and Schematic

The HP application note AN 1178, artwork Gerber file, schematic and a detailed materials list, etc. are available via the HP web site: www.hp.com/go/fiber.

Figure 4 shows the complete 622 MBd 1 x 9 multimode or single-mode fiber optic transceiver/SerDes/framer reference design circuit.

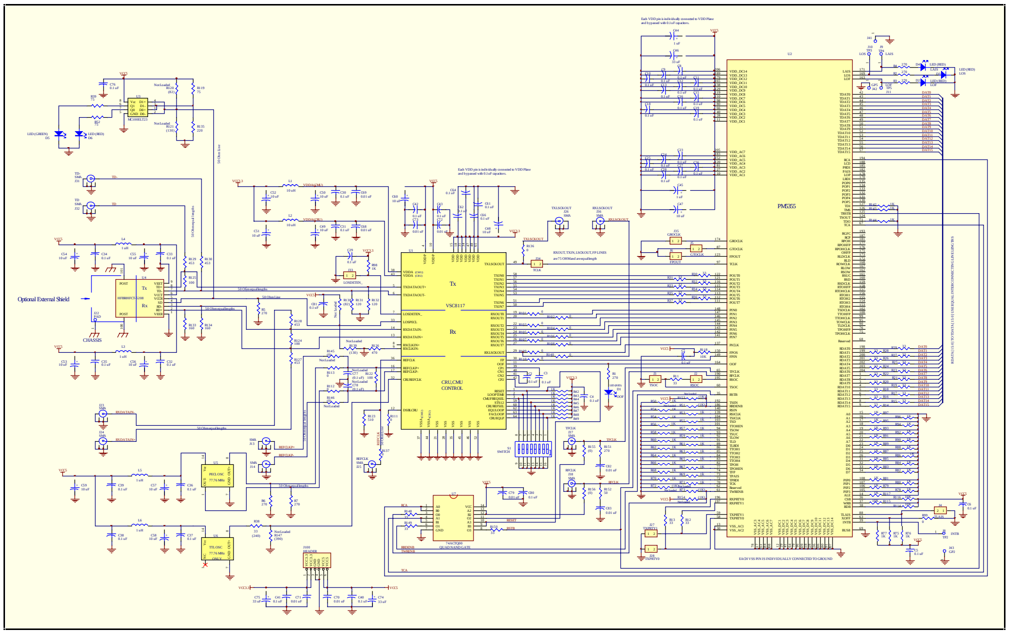


Figure 5-4 622 MBd 1 x 9 HFBR/HFCT-5208M/VSC8117/PM5355 Reference Design Schematic

Performance Data

This section presents measured results from the reference design board. The main measurement test points are shown in Figure 5. At each illustrated test point, the “where, what, and why” are explained to help understand the observed performance. It is hoped that this breakout of signal test points gives the designer a better appreciation of the individual as well as the combined performance of reference design components. Throughout the tests, typical components and normal operating conditions (room temperature, nominal power supply) were used. The results given in this section will represent what a designer typically should see when measuring an actual interface circuit board. Worst-case conditions or devices were not used for measurement in this section.

The main test data patterns used for the measurements were 1) a continuously repeating 622.08 Mb/s STS-12 pattern with PRBS 2^7-1 payload or 2) a SONET/SDH STS-12 pattern with a payload of scrambled ATM cells. The STS-12/PRBS pattern is 77,760 bits in length.

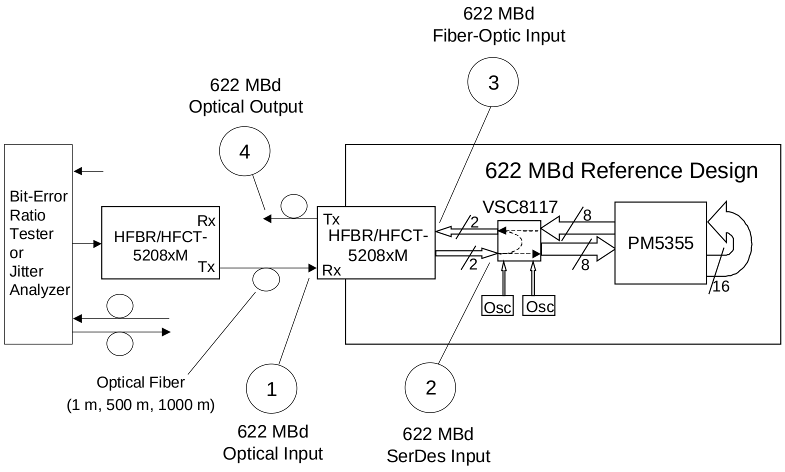


Figure 5-5 Block Diagram of Measurement Test Points for the 622 MBd Reference Design

Test Point 1: Optical Stimulus Waveforms

Waveforms of the optical sources used to test the reference design board are shown below in Figures 6, 7, and 8. The three optical waveforms for the 62.5/125 µm multimode fiber illustrate the effects of fiber dispersion upon the optical signal (longer rise/fall times, less amplitude with increasing length). The three multimode waveforms include the optical losses from the fiber optic attenuator, various connector adapters and splitter used in the test system, approximately 4 dB total loss.

Figures 9 and 10 show waveforms of the single-mode optical source over 1 m of single-mode fiber: Figure 9 shows a waveform without a 622 Mb/s SONET/SDH filter and Figure 10 shows the waveform with the 622 Mb/s SONET/SDH filter along with a mask template. In general, single-mode waveforms are measured with a standard SONET/SDH 622 Mb/s filter to eliminate the turn-on relaxation oscillation natural to the laser source dynamic response.

The 622 Mb/s OC-12 SONET/SDH filter is a fourth-order, Bessel-Thompson filter that has a –3 dB bandwidth of 467 MHz (0.75 x bit rate). Note that the shape of the output optical waveform indicates that the serial input signal provided to the fiber optic transmitter is properly terminated and replicated in optical form. The 622 MBd ATM-SONET/SDH standard defines an optical eye opening mask test that must be met by the fiber optic laser transmitter.

Figure 10 displays a typical HFCT-5208M transmitter optical waveform and the 622 MBd ATM-SONET/SDH eye-mask using 1 m of single-mode fiber cable and transmitting the STS-12 test pattern. This mask test has an added mask margin measurement shown. The margin amount is 25 percent larger than the required mask area. This additional margin area makes it more demanding for the optical waveform to meet the larger keep-out areas. No violations or “hits” resulted within the eye-mask template and its margin areas. This result provides more performance capability for the designer to use.

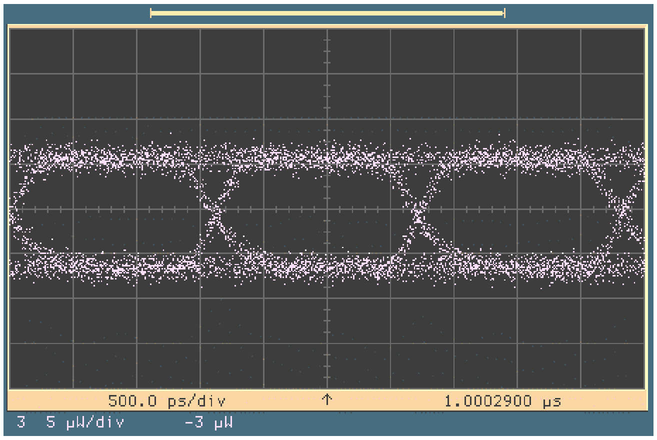


Figure 5-6 Input Optical Waveform with 1 m of 62.5/125 µm Multimode Fiber

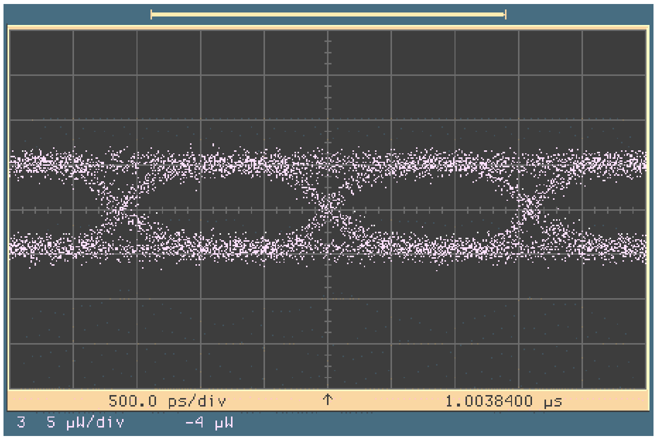


Figure 5-7 Input Optical Waveform with 500 m of 62.5/125 µm Multimode Fiber

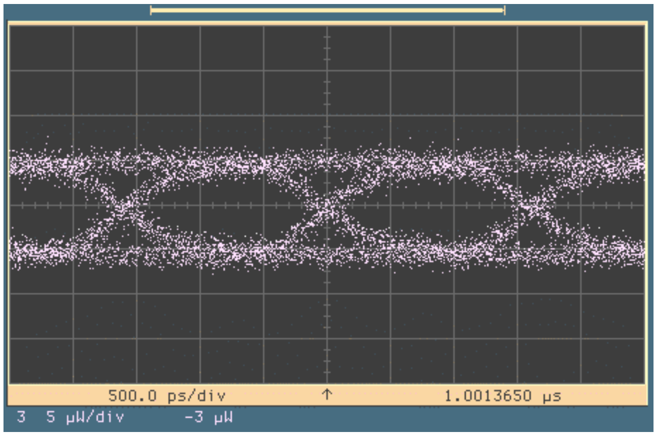


Figure 5-8 Input Optical Waveform with 1000 m of 62.5/125 µm Multimode Fiber

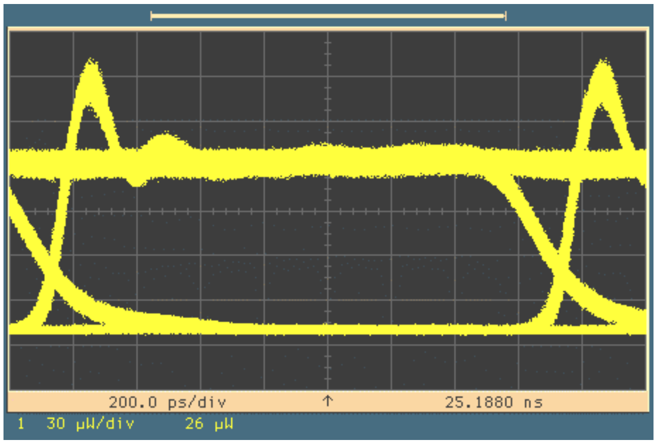
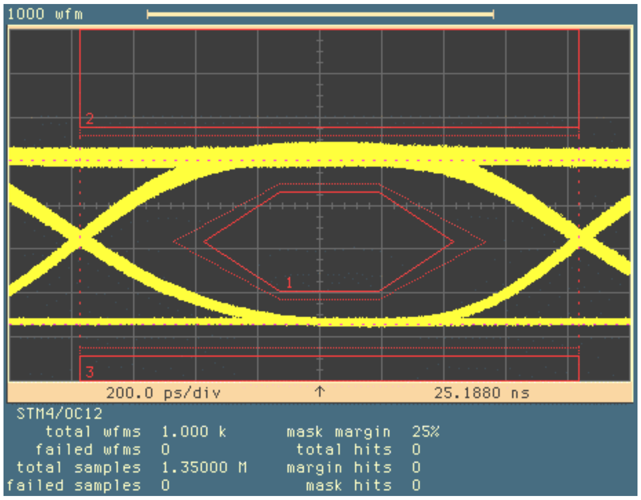


Figure 5-9 Input Optical Waveform with 1 m of Single-Mode Fiber Without an OC-12 Filter



```
 STM4/OC12
    total wfms  1.000 k       mask margin  25%
   failed wfms  0              total hits  0
 total samples  1.35000 M     margin hits  0
failed samples  0               mask hits  0
```

Figure 5-10 Input Optical Waveform with 1 m of Single-Mode Fiber with the SONET/SDH OC 12 Filter and Mask with An Additional 25 Percent Margin

Test Point 2: SerDes Serial Input Data Waveforms

At Test Point 2, waveforms were measured for Data and Data-bar individually and then together differentially for the SerDes VSC8117's serial data inputs. The HFBR-5208M fiber optic receiver Data/Data-bar outputs supply the signals via 50 Ohm transmission lines to the differential 100 Ohm load termination that is across the VSC8117's inputs. The input optical power to the receiver is set at two conditions: the highest optical power available from the test system and at the minimum sensitivity specification of –26 dBm average for this product to meet the multimode 622 MBd ATM-SONET/SDH standard requirement.

For example, at the highest available input optical power level (P_R) to the receiver of P_R = –22.0 dBm average while using 500 meters of typical 62.5/125 µm fiber, the single-ended Data eye opening is wide. For this condition, the typical signal-edge jitter is 300 ps peak-to-peak per the oscilloscope's accumulated sample data (~113 khits). When the input optical power is lowered to the minimum receiver sensitivity specification of PR = –26.0 dBm avg, per the multimode 622 MBd ATM-SONET/SDH standard, the total Data-edge jitter increases to 400 ps p-p (~108 khits). This 400 ps jitter is well within the standard's allowed total edge jitter of 1298 ps peak-to-peak.

Figures 11, 12 and 13 show respectively the Data, Data-bar and differential Data eye openings at the SerDes data inputs for the input optical power level of –26 dBm average The waveforms were measured with an approximate 10:1 resistor divider that is completed by a 50 Ohm input to a high-speed, sampling scope (20 GHz bandwidth). Figures 11, 12 and 13 show clean, wide eye opening waveforms that have negligible signal reflection effects in them. Table 1 shows total data jitter measured at PR = –26 dBm average by histogram method and "Tub" method vs. fiber optic link length.

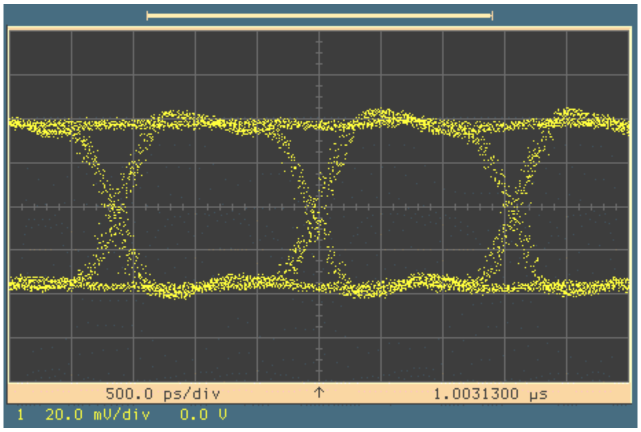


Figure 5-11 SerDes Serial 622 MBd Data Input with 500 m of 62.5/125 µm Fiber and at P_R = –26 dBm avg.

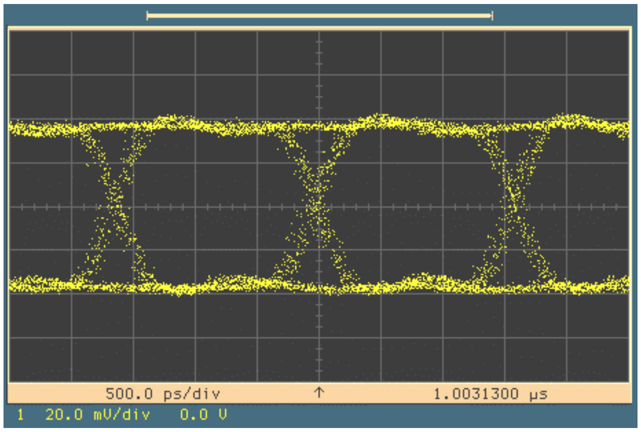


Figure 5-12 SerDes Serial 622 MBd Data-bar Input with 500 m of 62.5/125 µm Fiber and at P_R = –26 dBm avg.

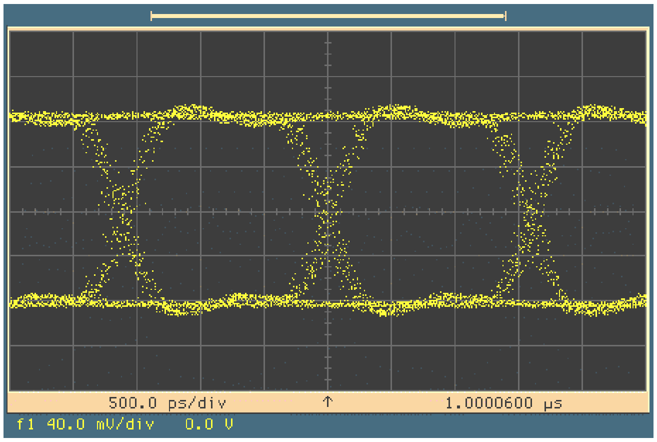


Figure 5-13 SerDes Serial 622 MBd Differential Data Input with 500 m of 62.5/125 µm Fiber and at P_R = –26 dBm avg.

Table 1. Total Data Jitter Measured at P_R = –26 dBm avg. by Histogram Method and "Tub" Method Versus Fiber Optic Link Length.

Link Length meters	**Total Data Jitter (Histogram) P_R = –26 dBm average ps p-p**	**Total Data Jitter (Eye Closure at BER=10^{-10} from Figure 14) P_R = –26 dBm average ps p-p**	**Total Data Jitter ANSI T1.646a MMF Standard ps p-p**
1	378	463	N.A.
500	400	489	1298
1000	433	532	N.A.

N.A. = Not Applicable

While a sampling oscilloscope provides a convenient way to measure jitter of signal waveforms on a sampled basis, a more accurate method is to check bit-for-bit error performance using a Bit Error Ratio Tester (BERT). The BERT can be used to develop unique data to help better quantify the jitter performance of a circuit. To use a serial BERT, the Data output from the fiber optic receiver is connected to the BERT as well as to the SerDes input. This connection allows measuring the sensitivity of the fiber optic receiver (P_R) as a function of the BERT's receiving clock time position ($t_{sampling}$) within the Data eye opening for a constant BER condition. When P_R versus $t_{sampling}$ is plotted, the graph is referred to as a "tub" diagram due to its U-shape appearance. In Figure 14., four different curves are given; the three BER = 10^{-10} curves of different fiber cable lengths are derived from a linear regression of higher error-rate data points. The fourth BER = 10^{-6} curve is actual measured values for the 500 metre length of cable. Of the four curves, three different 62.5/125 µm multimode fiber lengths are shown: 1 m, 500 m and 1000 m. The fourth curve of BER = 10^{-6} for 500 m length is used as a quick reference curve to estimate receiver performance without involving lengthy test time. The typical dB difference in the fiber optic receiver Input Optical Power between BER of 10^{-6} and BER of 10^{-10} for a 500 m link is approximate 1.6 dB at center of the bit interval. How to measure "tub" diagrams is explained later in the *Test Methods* section.

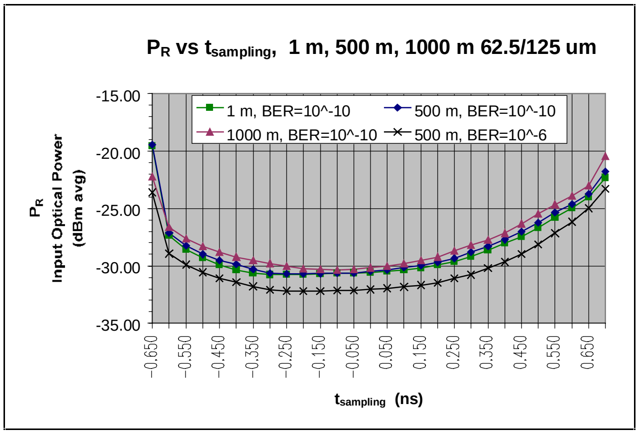


Figure 5-14 Optical Power (P_R) Versus Clock Sampling Time Position ($t_{sampling}$) at Constant BER of 10^{-10} and 10^{-6} for 1 m, 500 m and 1000 m Links "Tub Diagrams"

The interesting and informative nature of the tub diagrams is that one figure shows the eye opening time amount of a data signal for a given input optical power level to a fiber optic receiver at a required BER condition. The input optical power penalty (dB) can be seen easily if a wider data eye opening is needed for clock recovery circuit. Since this is a bit-for-bit error measurement, the converse of eye opening can be determined, i.e., the amount of eye-closure or the total jitter that is occurring on the signal at a specific BER condition. The wider the U-shape tub, the better the eye opening performance of the fiber optic receiver. The deeper the U-shape tub, the more sensitivity the receiver is for using less input signal level. Any asymmetry in the U-shape can point to possible design or performance issues. The "tub" diagram is quite an informative figure.

Estimation of SerDes's Input Clock Recovery Eye Opening Requirement

In the multimode 622 MBd ATM-SONET/SDH standard, the smallest allowable data eye opening time for the SerDes clock recovery unit to operate within is 310 ps. This is referred to as a time "window" opening needed by the SerDes to recover the clock and retime the serial data without exceeding the required error rate for this application. The VSC8117 SerDes data sheet does not specify this parameter. The following test method and results give a realistic estimate of the actual clock recovery circuit's window opening value.

The VSC8117 SerDes is configured to operate in Facility Loopback mode (FACLOOP switch placed in the "off" position). This mode causes the 622 MBd serial data to loopback from the received data to the transmitted data. The BERT receives this transmitted serial data, and then compares the sent data with this returned data. When the BERT's receive clock is positioned at the center of the baud interval of the returning data, the input optical power to the fiber optic receiver is lowered to different levels to achieve different BER values. This data then is extrapolated by the linear regression technique described in the *Test Methods* section about measuring tub diagrams. A predicted value for the input optical power to the receiver is obtained for a BER of 10^{-10}. This SerDes retimed data error condition of 10^{-10} corresponds to a fully-jittered, or closed retimed data eye. This condition occurred because the input received data eye opening to the SerDes's input equaled the window opening needed by the clock recovery circuit for the BER of 10^{-10}. The input optical power level that caused the SerDes output to have a BER of 10^{-10} is the sensitivity level used to determine the eye opening from the corresponding tub curve for the received data at the SerDes input (at the same conditions of BER, cable length, etc.). It is assumed that the clock of the clock recovery circuit is positioned at the center of the baud or data interval. The resulting time width to the nearest edge of the tub curve is one-half of the clock recovery's window requirement in order to maintain a BER of 10^{-10}. If the clock position is not centered in the baud interval, then the true time position must be known to determine the actual window time width for the clock recovery circuit with this technique. The following specific example shows an estimate for the window time width of the VSC8117 clock recovery circuit. Refer to Figure 15, Table 2, and Figure 16, for the tub diagram data described below.

The SerDes's clock recovery window-opening test was done using the 622 MBd reference design circuit. The test conditions including the use of a 1000 meter length of 62.5/125 µm fiber optic cable, theVSC8117 SerDes is in Facility Loopback mode and the BERT clock is positioned in the center of the retimed serial data output eye opening. The bit error rate is measured as a function of the fiber optic receiver sensitivity. The BER values were extrapolated to BER of 10^{-10} and the corresponding input optical power was found to be $P_R = -30$ dBm avg. From the 1000 m/BER = 10^{-10} tub curve, Figure 16, which represents the received data eye opening to the SerDes's input, and assuming that the SerDes's recovered clock position is at the center of the baud interval, the corresponding eye opening is then twice the 50 ps time interval to the nearest edge (right side) of the tub curve. The estimated clock recovery window time width is approximately 100 ps. This is an estimated value because if the SerDes's recovered clock position is to the left of center, then the window time width would be larger. For example, if the clock position was 100 ps to the left of center, then the window time width could be approximately 300 ps. If the clock position is any further to the left, the window would become smaller again. Also, at this $P_R = -30$ dBm average level, and if the recovered clock position was to the right of center interval by 50 ps, the window time width becomes essentially zero which is unrealistic. Hence, the most likely estimate for the recovered clock window time width is between 100 ps to 300 ps. The range of values meets and is within the multimode 622 MBd ATM-SONET/SDH standard's minimum data eye opening amount of 310 ps that can be provided to the SerDes for it to meet or exceed the standard's BER of 10^{-10}.

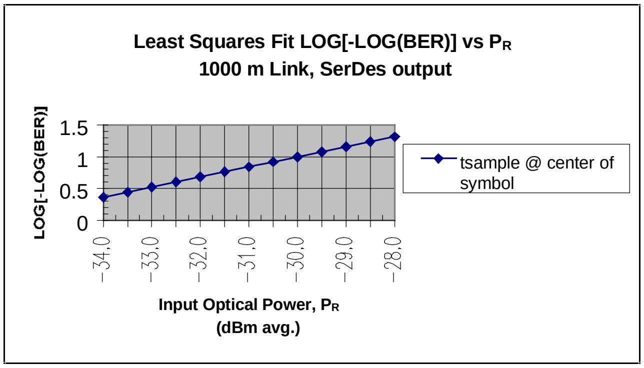


Figure 5-15 Least Squares Fit of Log(-Log(BER)) Versus Input Optical Power (P_R) for Center of Symbol from SerDes Output with1000 m 62.5/125 µm Fiber Optic Link

Table 2 Conversion Between BER and LOG[-LOG(BER)] Values

BER	LOG [-LOG(BER)]
10^{-2}	0.3010
10^{-3}	0.4771
10^{-6}	0.7782
10^{-9}	0.9542
10^{-10}	1.0000
10^{-12}	1.0792

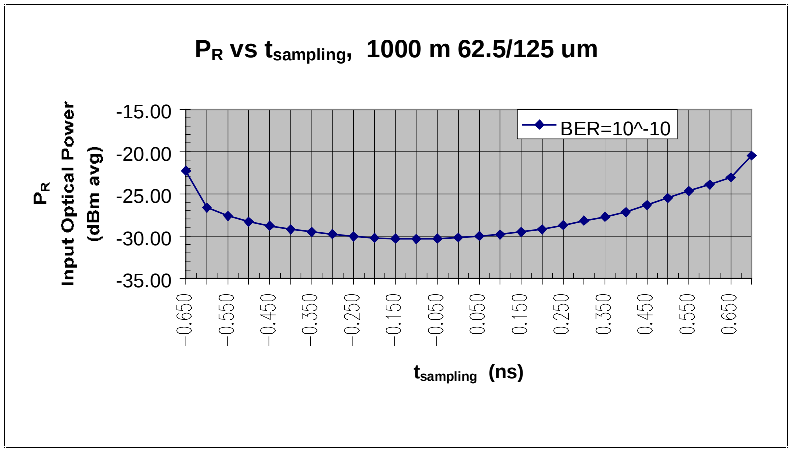


Figure 5-16 Receiver Input Optical Power (P_R) Versus Clock Sampling Time Position ($t_{sampling}$) for Constant BER = 10^{-10} for 1000 m Link

Test Point 3: Fiber Optic Transmitter Input Data Waveforms

The transmitter input waveforms are of good signal fidelity, showing minimal reflections. The waveforms are shown in Figures 17 (Data), 18 (Data-bar), and 19 (Data–Data-bar) for a 500 m length of 62.5/125 m fiber and with the fiber optic receiver input optical power adjusted to P_R = –26.0 dBm average. For example, the total Data edge jitter measured at Test Point 3 is 233 ps p-p for ~112 k-samples. It is interesting to note that the SerDes's output total Data edge jitter did not change significantly in its peak-to-peak value of approximately 211 ps to 233 ps when either the 1 m, 500 m, or 1000 m of multimode fiber was used in the link prior to the SerDes IC. The SerDes was in Facility Loopback mode (serial data loopback). Basically, the SerDes output data jitter was not affected by input signal jitter to the SerDes device. This is due to the good clock recovery/data retiming circuit performance within the SerDes unit and the low-jitter fiber optic receiver performance.

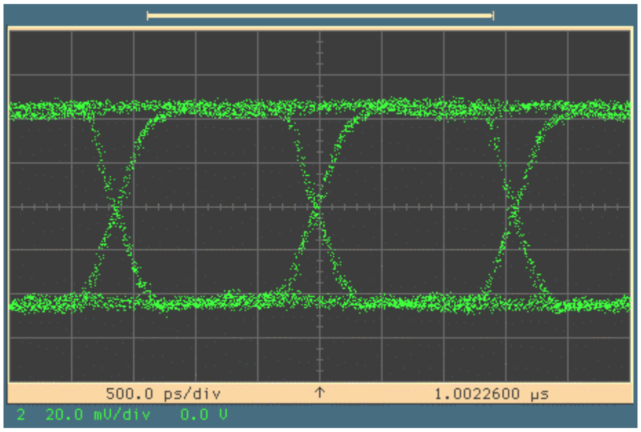


Figure 5-17 HFBR-5208M Transmitter Serial Data Input with 500 m of 62.5/125 µm Fiber and at P_R = –26 dBm avg. with the SerDes in Facility Loopback Mode

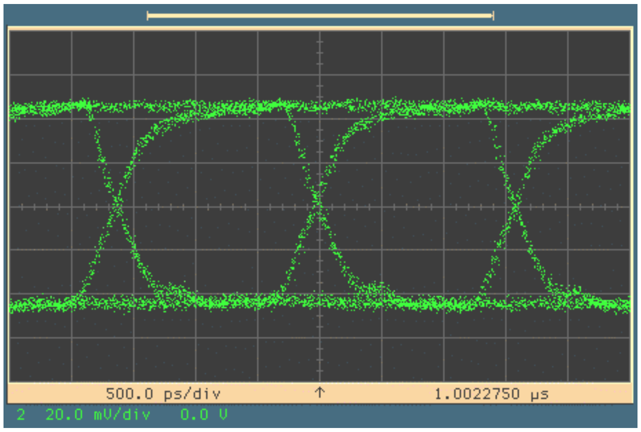


Figure 5-18 HFBR-5208M Transmitter Serial Data-Bar Input with 500 m of 62.5/125 µm Fiber and at P_R = –26 dBm avg. with the SerDes in Facility Loopback Mode

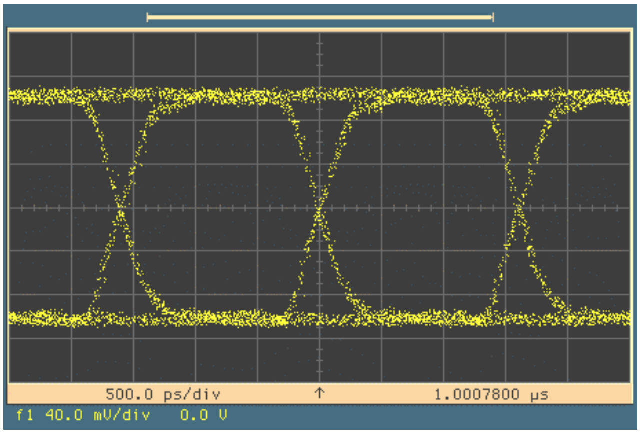


Figure 5-19 HFBR-5208M Transmitter Serial Differential Data (Data – Data-Bar) Input with 500 m of 62.5/125 µm Fiber and at P_R = –26 dBm avg. with the SerDes in Facility Loopback Mode

Test Points 1 to 4: Jitter Tolerance, Jitter Transfer, Jitter Generation Tests

PMC-Sierra, Inc., is currently confirming proper operation of the 8-bit and 16-bit bus interconnections between VSC8117 and PM5355. In addition, frequency-based jitter tests with 622.08 Mb/s ATM-SONET/SDH patterns are in progress. Data will be reported when it becomes available from PMC-Sierra.

Test Methods

Guidance on Testing Methods

This section explains common techniques used for directly testing and measuring performance of the 622 Mb/sec components on the reference design board.

For testing the reference design board, serial data format is used because common test equipment is available for providing convenient test signals, observing high-speed waveforms and measuring BERs. Various fiber cable lengths are tested to show the effects of optical signal dispersion* in a fiber. Note, however, there are many factors that can degrade a signal in a communication link. The purpose is to explain how to practically measure and quantify the effects relating to the 622 Mb/sec standards.

One of the most important parameters that demonstrate how well a serial link is performing is the quality of the data eye opening. There are related and measurable parameters that quantify the data eye opening performance for a serial link. They are the time-based jitter of the signal measured by a histogram method. Also, time-based jitter can be observed by measuring the input optical power to the receiver as a function of time position within the data eye opening for a constant BER condition. As described in detail earlier, this data plotted as a graph is called a “tub” diagram. An eye-mask template measurement of the transmitter output optical power can be measured as well. Specific data for the types of parameters was shown for various conditions in the section entitled, *Performance Data*.

Data Jitter Histogram

Measurement of time-based data jitter is done by using a very high-speed sampling oscilloscope, such as the 20 GHz HP83480A with its electrical or optical plug-ins. This instrument can develop a histogram of the data jitter that is defined by both a proportion of the signal amplitude and baud time interval centered at the mid-level of the data transition crossings. Some sampling scopes have internal algorithms that automatically measure the data jitter in peak-to-peak or rms values as well as other automatically measured parameters. The trigger for the scope is the highest speed clock that runs the system. The data jitter is not only dependent upon the “threshold window” of voltage and time, but upon the amount of waveform samples taken (or measurement time) and the type of data pattern used for the test.

Measure Receiver Sensitivity Versus $t_{sampling}$ (Tub Diagram)

Measurement of time-based jitter of the fiber optic receiver by observing the input optical power (P_R) level needed versus the time position within the eye opening to maintain a constant BER condition ("tub" diagram). This is a more involved test. However, this test is very informative and provides an accurate, bit-for-bit error measurement to determine the eye opening (or total jitter) over a wide range of P_R levels. The basic measurement technique to create a tub diagram is to sample the returning serial data to the BERT with a BERT clock phase-shifted over the usable data eye opening without losing synchronization. At each measured time-position, record P_R at BER levels of 10^{-4}, 10^{-5}, 10^{-6}, and 10^{-7}. This BER data is extrapolated by linear regression on a log(-log) scale versus a linear P_R scale that allows a prediction of P_R at the required operating level of BER = 10^{-10} or better. From this graph, the data eye opening time can be determined at any P_R level of interest.

Measure ATM-SONET/SDH Frequency-Based Jitter

(Information to be supplied by PMC-Sierra for testing Jitter Transfer, Jitter Tolerance and Jitter Generation.)

Eye Mask Measurement

Measurement of an eye-mask waveform is straight forward and is done by using the high-speed sampling scope's built-in mask template and an appropriate bandwidth filter for the 622 MBd ATM/SONET/SDH standard. The eye-mask test pertains only to the output optical waveform from the single-mode fiber optic transmitter. The HP83486A 2.5GHz 1300 nm optical-to-electrical plug-in for multi-mode and single-mode fiber works well for performing this test.

* Optical signal dispersion causes the optical signal to spread out over a baud interval which ultimately will cause more jitter in a link and limit the signaling rate for a given length of fiber cable. Optical dispersion is caused by both modal dispersion (different light modes arrive at different times at the end of the fiber) or chromatic dispersion (different wavelengths arrive at different times at the end of the fiber) in multimode fiber. In single-mode fiber only, chromatic dispersion is an issue.

Test Configurations

A recommended test configuration for evaluating the 622 MBd OC-12 reference design is shown in Figure 20. This test setup uses standard, high-speed test instruments such as a BERT, a sampling oscilloscope and a programmable delay generator. Fiber optic test equipment needed to measure the reference design performance are a fiber optic attentuator, optical power meter, an optical-to-electrical converter (O-E), a 70 percent/30 percent fiber optic splitter, fiber optic cable, and another evaluation board to provide an equivalent BERT signal in optical form. When using the 1300 nm LED-based HFBR-5208M transceiver, multimode fiber and test equipment are used. When using the 1300 nm laser-based HFCT-5208M transceiver, single-mode equipment is used.

The recommended sampling oscilloscope, HP83480A, has plug-ins for 1300 nm single-mode fiber (HP83485A) and for 1300 nm multimode fiber (HP83486A). The plug-ins are effectively an O-E converter, an optical power meter and a waveform analyzer combined into one unit. Some general comments about fiber optic transceiver testing are listed below.

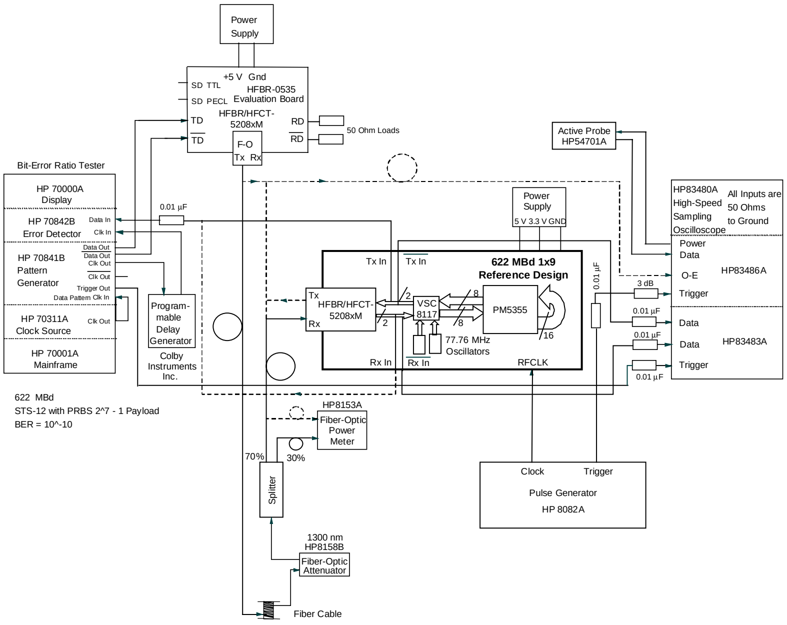


Figure 5-20 Block Diagram of the 622 MB/s Test System

Signal Monitoring

Monitoring the active 622 Mb/s serial data signal between the fiber optic transceiver and the SerDes unit without affecting the signal is done with an approximate 10:1 voltage divider circuit. This is a convenient method to observe the signal while using high speed 50 Ohm input test equipment, such as the high-speed HP83480A sampling scope or the HP70000 series BER Tester. Use of a high-impedance active probe in place of the resistive voltage-divider circuit, will not provide as large a measurement bandwidth (2.5 GHz) as does an oscilloscope 50 Ohm input circuit (20 GHz). In addition, the active probe is mechanically less convenient to use. The reference design on-board divider is made of a 453 Ohm surface-mount resistor that connects to monitor the signal line. A 50 Ohm transmission line trace connects at one end to this resistor and at the other end of the line connects to a SMA connector that, in turn, connects to 50 Ohm coaxial cable to the 50 Ohm input of the scope. When connecting this resistive divider to the BER Tester serial data input, an in-line 0.01 µF blocking capacitor should be used to remove the small (÷10) dc bias that exists on this line. Both sets of transmit and receive differential data lines have the resistive divider monitoring capability.

Avoiding Test Pitfalls

Here are a few pitfalls to avoid when testing with this evaluation board and its components.

- When using the HP70000 series BER Tester with a low-level PECL input signal, such as from the 10:1 resistive divider circuit, the typical minimal signal level the BERT can use is about 60 mV p-p. The 10:1 attenuator circuit provides approximately 80 mV p-p which is adequate to operate the BERT.
- If an optical power splitter is used with a 622 MBd fiber optic transmitter in the test setup for measuring a tub diagram, use a 70 percent/30percent optical splitter with low insertion loss to provide a useable optical power range for the fiber optic receiver.

Test Equipment

Table 3. List of Suggested Test Equipment

Title	Manufacturer	Model Number	Quantity	Notes
Digital Communication Analyzer	Hewlett-Packard	HP83480A	1	3
Optical/Electrical Module (O-E Plug-in)	Hewlett-Packard	HP83486A with Optional OC-12 filter	1	1; One channel is for 1300 nm multimode light, one electrical channel is 20 GHz
Optical/Electrical Module (O-E Plug-in)	Hewlett-Packard	HP83485A	1	1; One channel is for 1300 nm single-mode light, one electrical channel is 20 GHz
Electrical Module (Plug-in)	Hewlett-Packard	HP83483A	1	Two electrical channels with 20 GHz bandwidth
Bit-Error-Ratio Tester	Hewlett-Packard	HP70000 Series	1	2
Jitter & Eye-Diagram Analyzer	Hewlett-Packard or Tektronix	HP71501A Series or Tektronix SJ300	1	Automated measurements of SONET/SDH Jitter Tolerance, Transfer & Generation
Programmable Delay Generator	Colby Instruments, Inc.	CPDL	1	Delay up to 100 ns in 10 ps steps
Pulse Generator	Hewlett-Packard	HP8082A	1	Use an equivalent instrument to this if unavailable (obsolete)
Optical Power Meter	Hewlett-Packard	HP8153A	1	Use with two HP81533A plug-in modules
Optical Power Heads	Hewlett-Packard	HP81521B	2	Optical Heads necessary for HP8153A meter
Optical Attenuator	Hewlett-Packard or JDS	HP8158B option 002 & 011or JDS HA9	1	For multimode & single-mode fibers
Optical Splitter	Canstar (or equivalent)	MR4-B-62.5 10676	1	70%/30% split ratio for 62.5/125 μm fiber
Fiber optic Cables	Siecor; Red Hawk	Siecor TB-1KM-62-ST-SM (1 km); Red Hawk CD-97245-02 (500m);	1	62.5/125 μm multimode fiber
Power Supplies	Hewlett-Packard	HP6236B; HP E3601A	1 1	Triple Output, 6 Vdc/2.5 A, ±20 Vdc/0.5 A; Single Output, 8 Vdc/ 3 A or 15 Vdc/2 A
622.08 Mb/s Reference Design Board	Hewlett-Packard	Version 1.1	1	Test Circuit
1 x 9 Evaluation Board	Hewlett-Packard	HFBR-0535	1	Provides electrical to optical conversion
Mulitmode and Single-mode 1 x 9 Fiber Optic Transceivers	Hewlett-Packard	HFBR-5208xM HFCT-5208xM	2 2	Multimode Single-mode
Miscellaneous Wire and Fiber Optic Accessories	Hewlett-Packard; Picosecond Pulse Labs; Fiber optic connector suppliers: Amphenol, Red Hawk, Siecor	HP11742A 0.01 μF; PPLabs 5501A, 5502A 0.01 μF; HP8493A –3 dB, HP8493C –20 dB attenuators	Varies	SMA Coupling Capacitors, Attenuators, Terminations, SMA-connector Coaxial Cables; Fiber optic connector adapters

Test Notes

Optical-to-Electrical Converter—The optical performance was measured with a 1300 nm 2.5 GHz bandwidth optical-to-electrical converter. With this O-E converter plug-in for the HP83480A oscilloscope, the optical extinction ratio, rise/fall times, pulse-width distortion and jitter can be measured along with an eye-mask compliance test.

BERT—For receiver sensitivity test at the center of the data eye opening, the BERT can automatically self-align and sample the receiver output data at the center of the baud interval. For receiver sensitivity at the left or right of the center baud time position, then a programmable delay generator must delay the sampling clock edge to the appropriate time position within the eye opening.

HP83480A High-speed Sampling Scope—Measure extinction ratio automatically with this scope. Basically, the transmitter extinction ratio is equal to [Pon /Poff] 100% in percent or as 10log [Pon /Poff] in dB. A mask template can be custom configured or a pre-configured internal mask can be used. For convenience, an internal SONET/SDH OC-12 mask can be used for 622.08 MBd testing. The HP83480A 20 GHz scope can save data to memory for later non-real-time analysis or for storage to floppy disk file for documentation needs.

Conclusion

As seen from the information presented in this paper, designers can quickly use this proven, three-vendor developed, "standard compliant" reference design to create a 622.08 Mb/s, OC-12 ATM-SONET/SDH Physical Layer interface with Framer function. With a common electrical and mechanical interface for the fiber optic multimode and single-mode units, design changes to the circuit are minimal or not required when interchanging fiber optic interfaces. This gives flexibility to the design without modifying the SerDes and Framer circuitry.

In addition, the data that was measured from this reference design helps support the designer to achieve a working design on the first attempt. Test methods and configurations were given to help provide understanding of how best to check design performance. Also, guidance was provided to assist in printed circuit board layout and circuit design with the SerDes IC, the Framer IC, and the fiber optic transceivers. Unique information about the operation of the devices was also discussed. Armed with this guidance, designers can quickly and successfully develop a flexible 622 Mb/s OC-12 ATM/SONET/SDH Physical Layer interface with minimal time, resources, and expense.

References

A full complement of reference data is available in HP Application Note, AN 1178, which can be found on the HP web site: www.hp.com/go/fiber.